

Essentials Oak 14 Schematic

Chief River

2012-09-05

REV : A00

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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

M14 DIS

DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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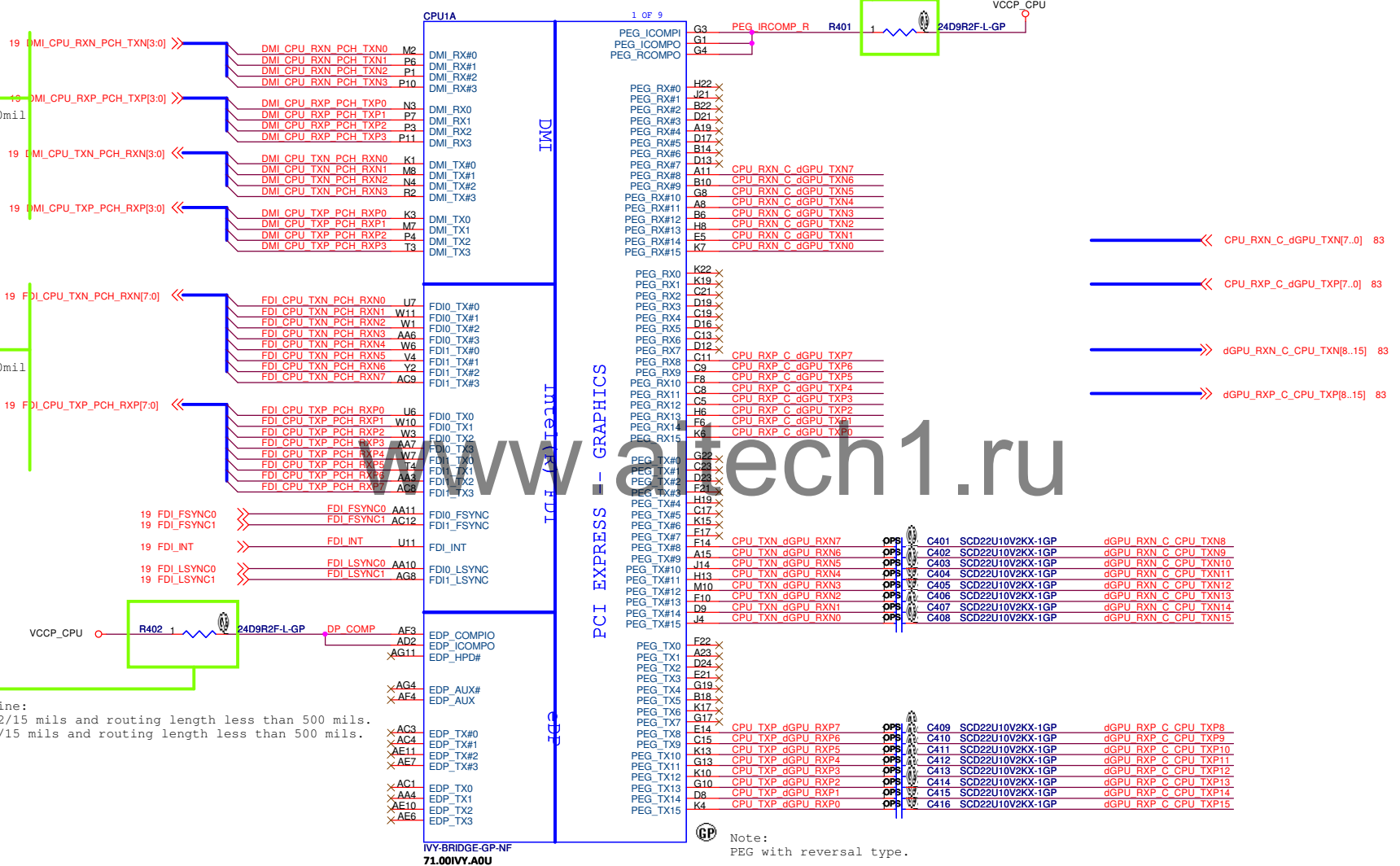
SSID = CPU

Layout Note:
DMI trace length 2000~8000mil

Layout Note:
FDI trace length 2000~6500mil

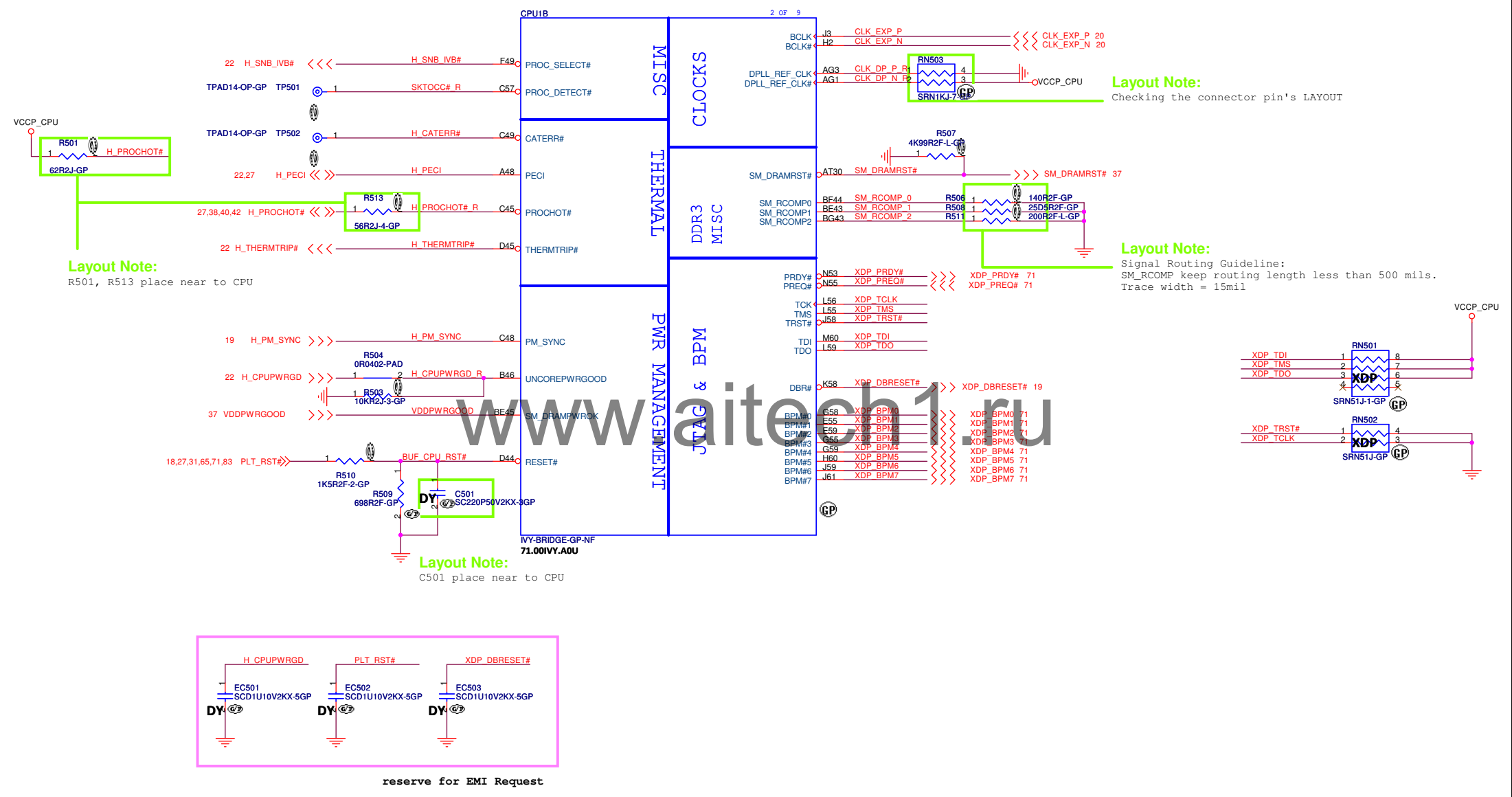
Layout Note:
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Layout Note:
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
PEG with reversal type.

SSID = CPU



Layout Note:

R501, R513 place near to CPU

Layout Note:

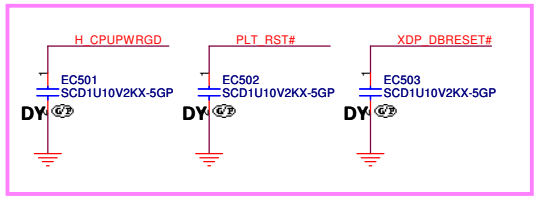
Checking the connector pin's LAYOUT

Layout Note:

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil

Layout Note:

C501 place near to CPU

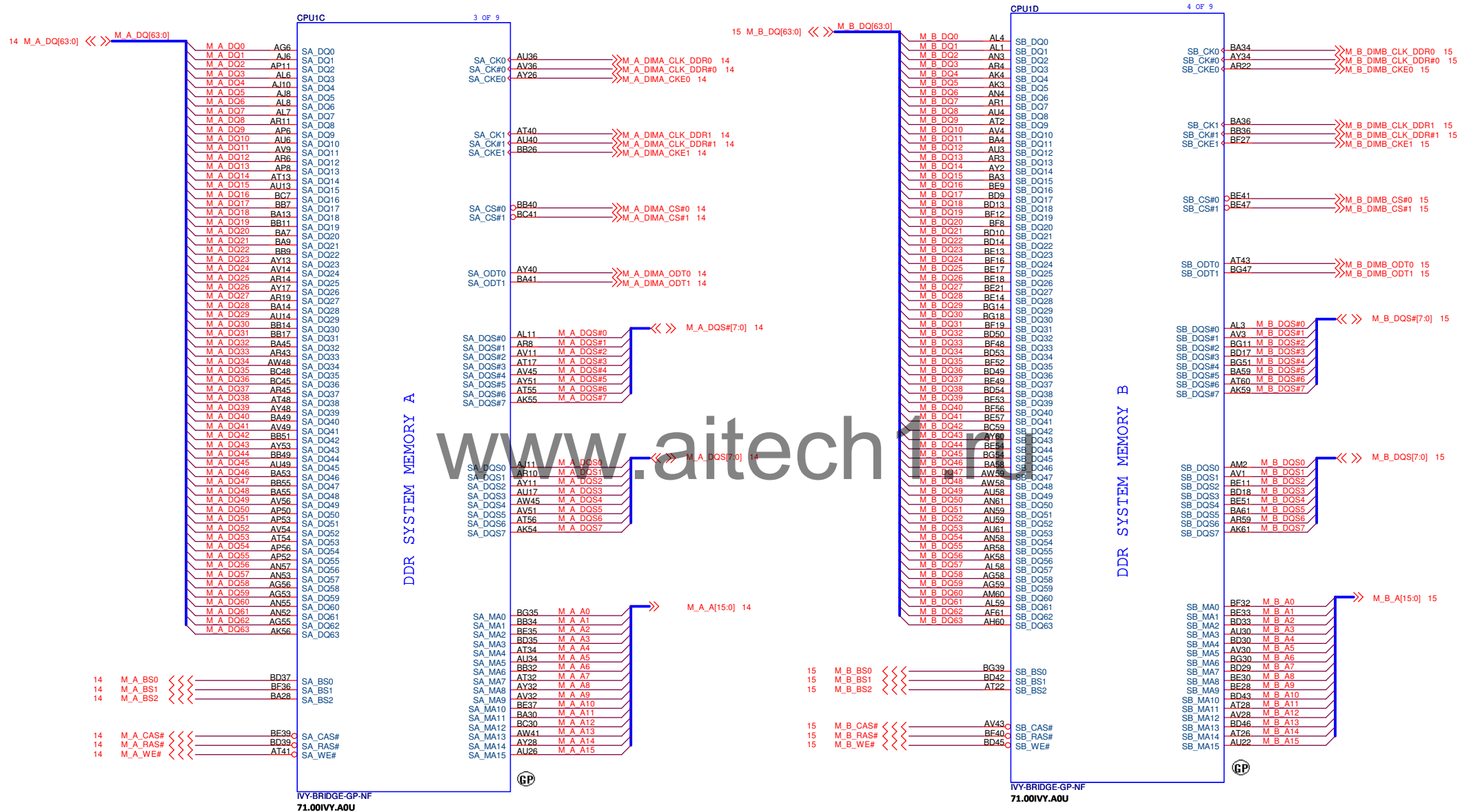


reserve for EMI Request

M14 DIS

DELL			Wistron Corporation		
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Title CPU(THERMAL/CLOCK/PM)					
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SSID = CPU



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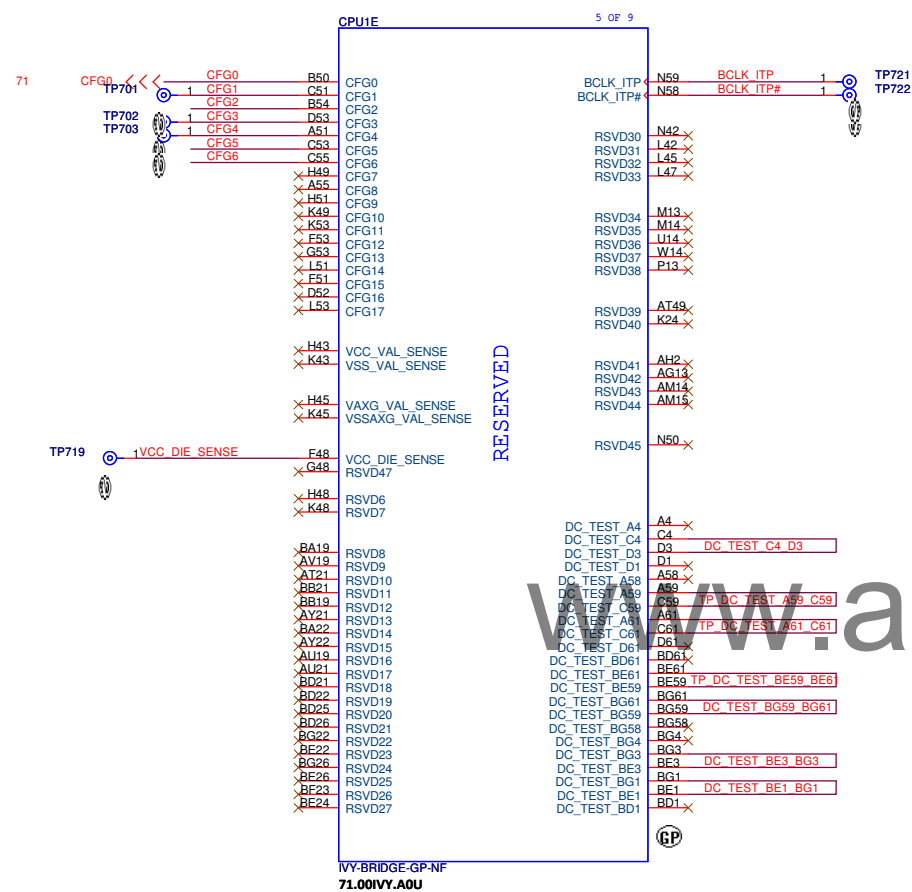
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SSID = CPU



PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

Display Port Presence Strap	
CFG[4]	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

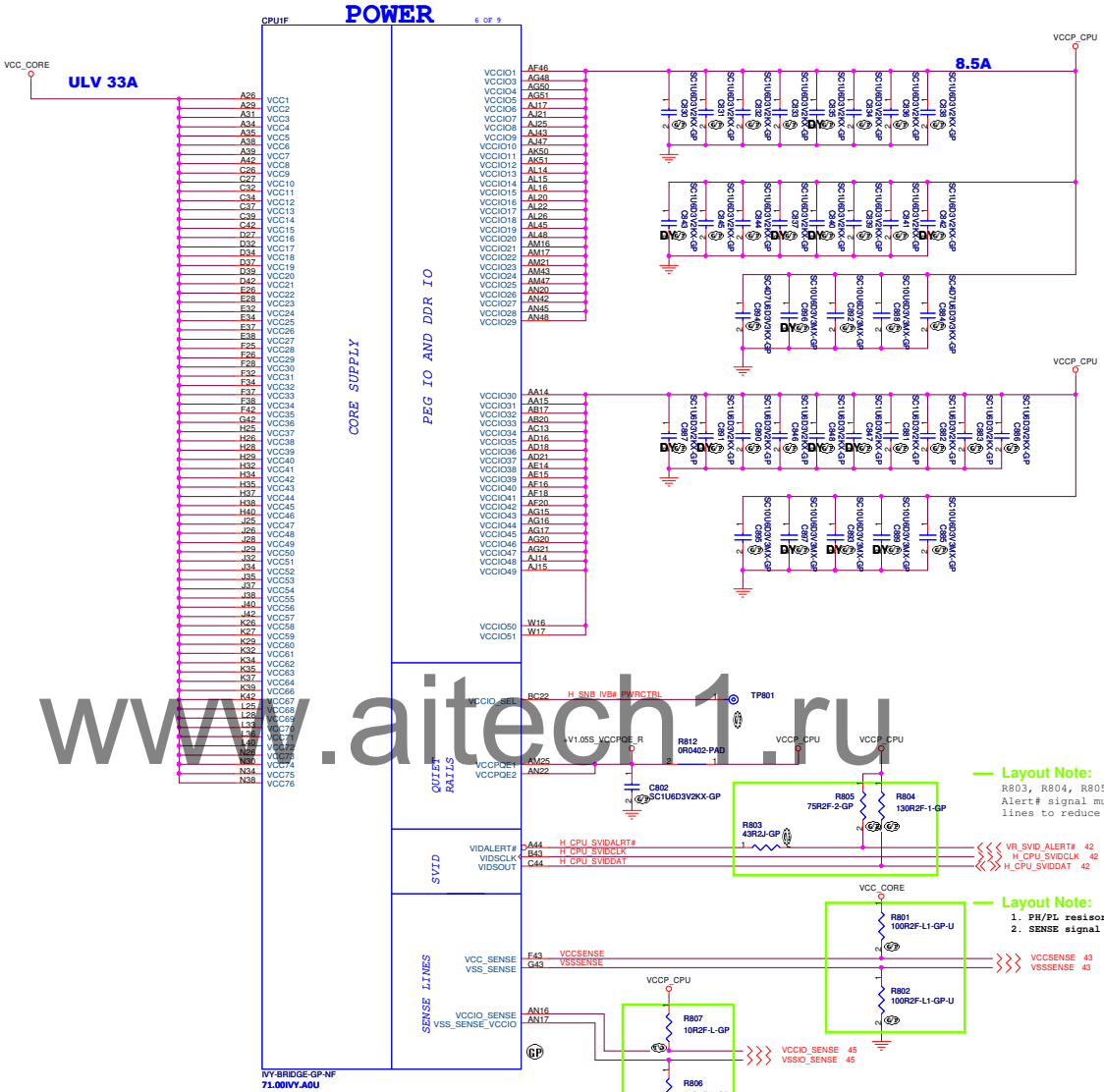
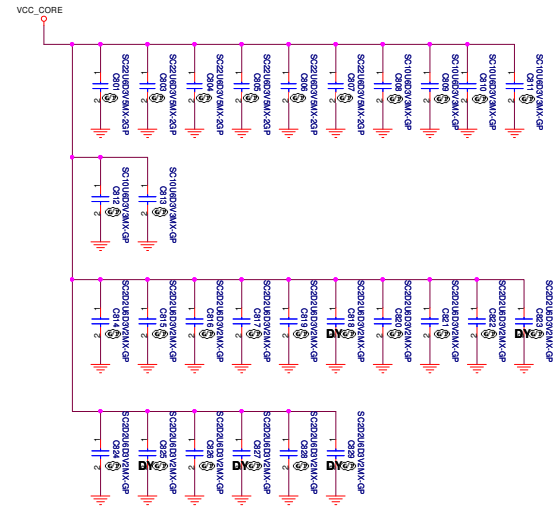
PCIe Port Bifurcation Straps	
CFG[6:5]	11: 1x16 PCI Express
	10: 2 x8 - PCI Express
	01: Reserved
	00: 1x8, 2x4 PCI Express



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CPU (RESERVED)			
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SSID = CPU



VCCPU Output Decoupling CAP Recommendation:
1 x 1 uF (0402)

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Need place Pull Hi at IMVP page

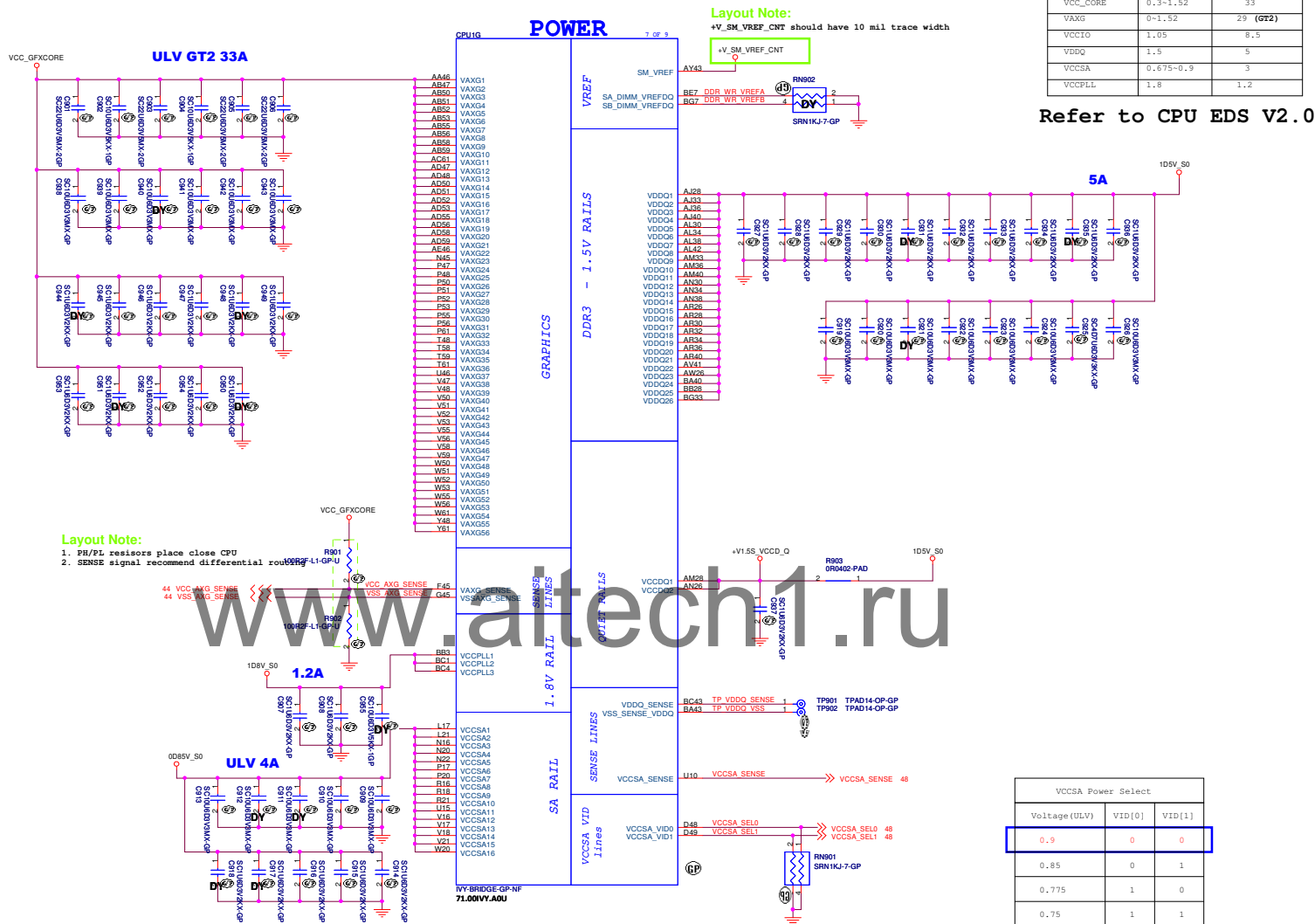
Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Layout Note:
1. PH/PL resistors place close CPU
2. SENSE signal recommend differential routing

Voltage Rail	Voltage (V)	Iccmax (A)
VCC_CORE	0.9~1.52	33
VAXG	0~1.52	29 (GT2)
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.675~0.9	4
VCCPLL	1.8	1.2

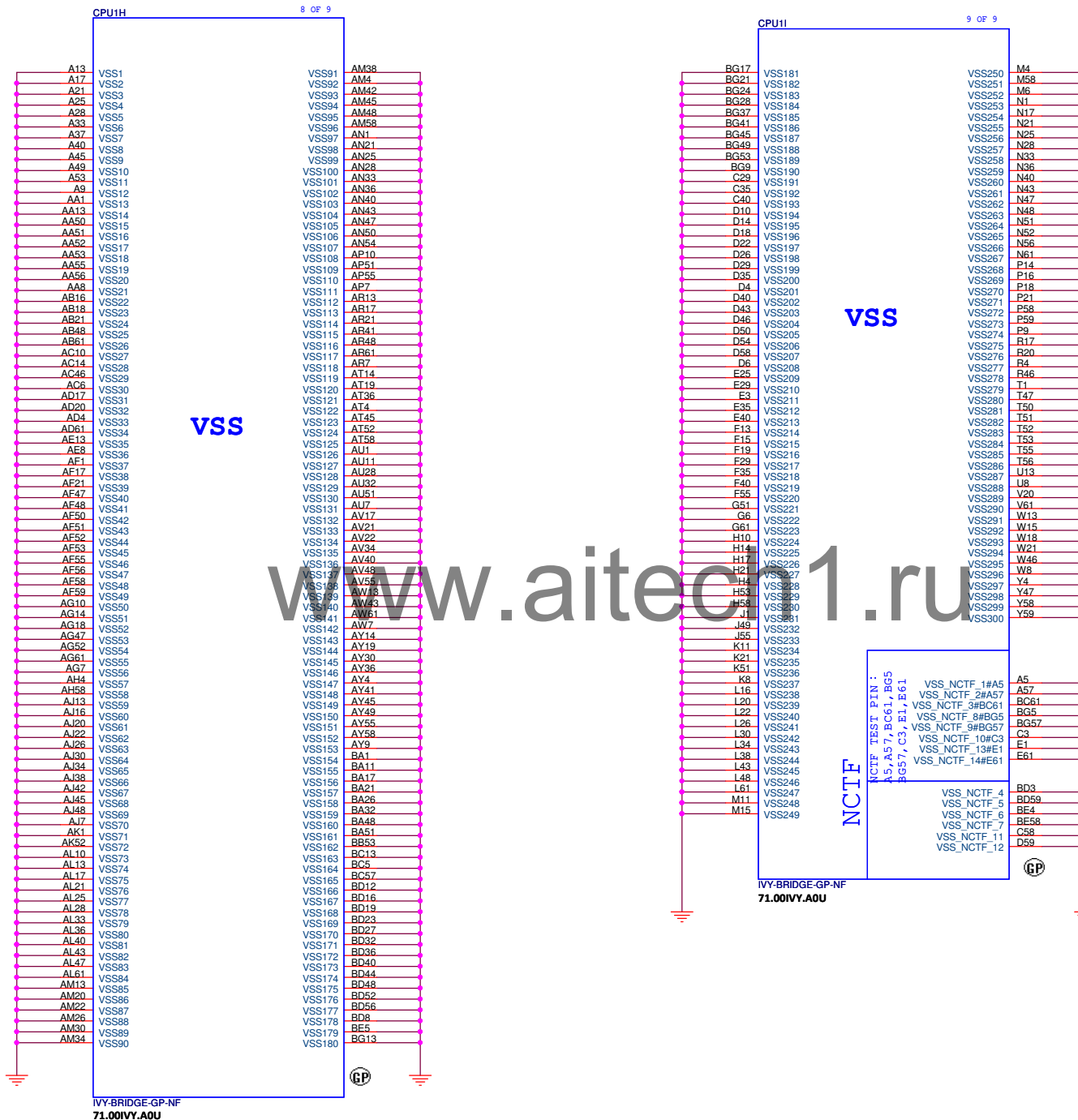
Refer to CPU EDS V.1.7.5

SSID = CPU



VCCSA Power Select		
Voltage(ULV)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

SSID = CPU



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CPU (VSS)Size
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XDP


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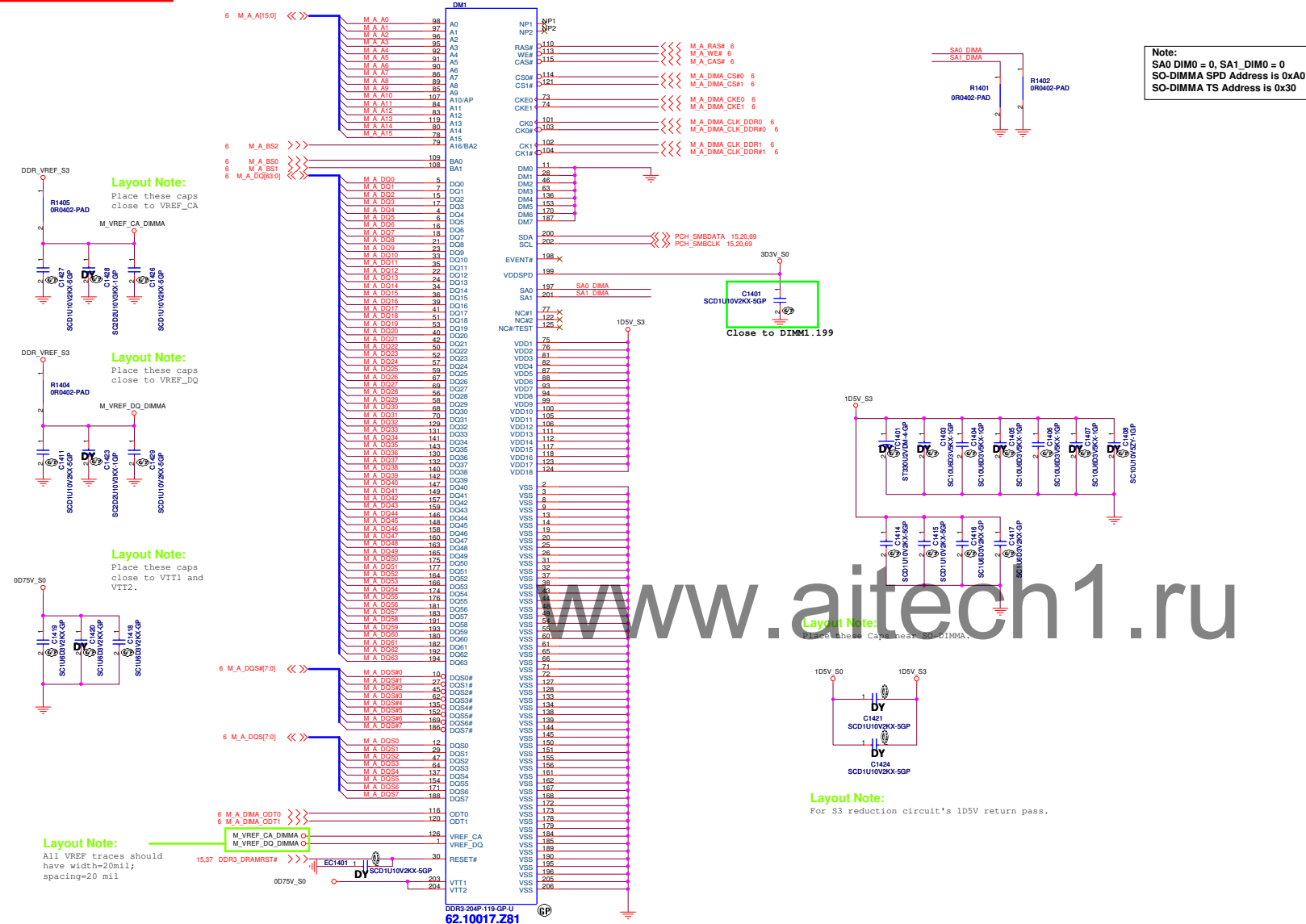
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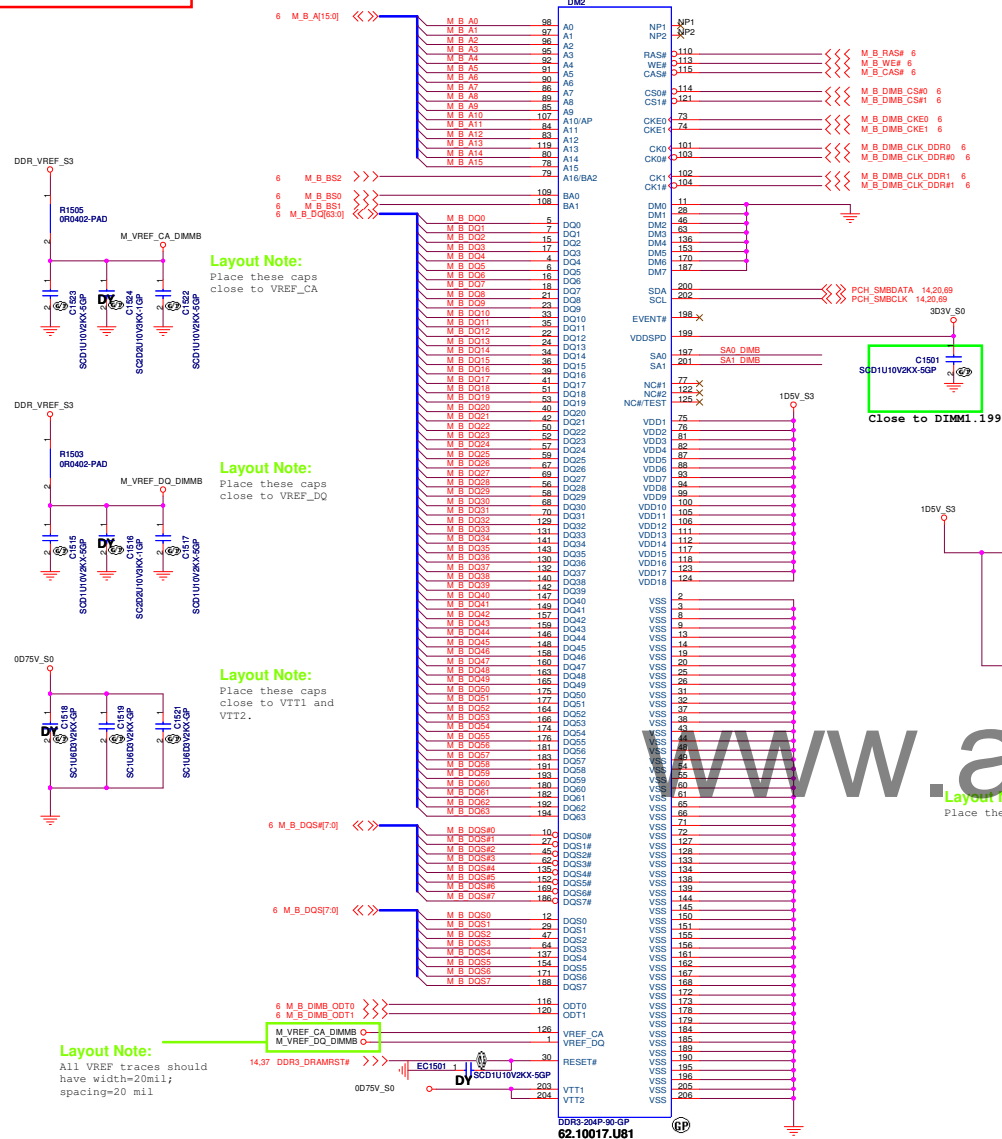
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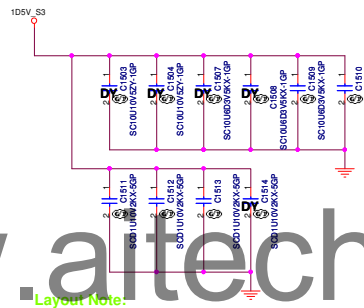
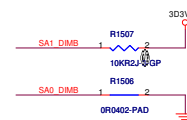
SSID = MEMORY



SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



Layout Note:
Place these Caps near SO-DIMM



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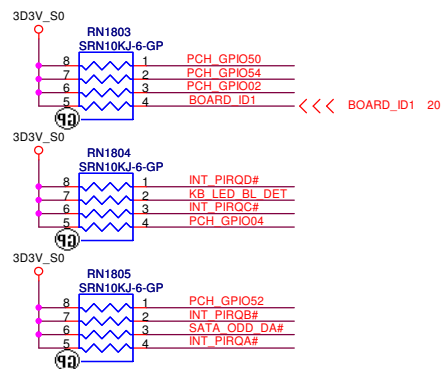
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Title			
PCH (LVDS/CRT/DDI)			
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SSID = PCH



USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

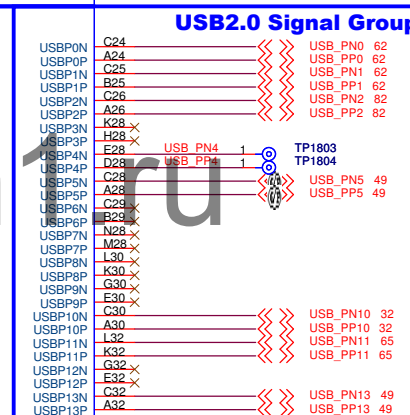
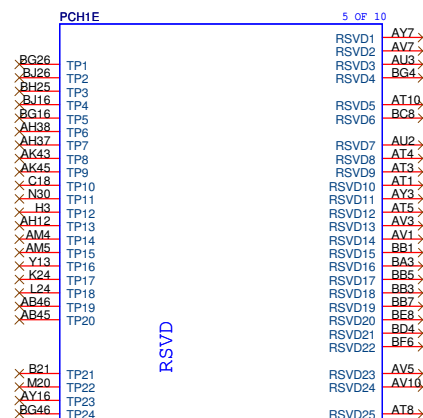
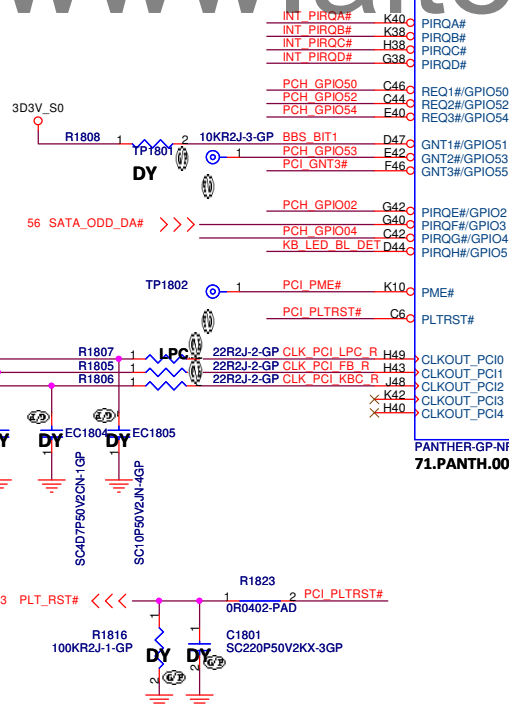
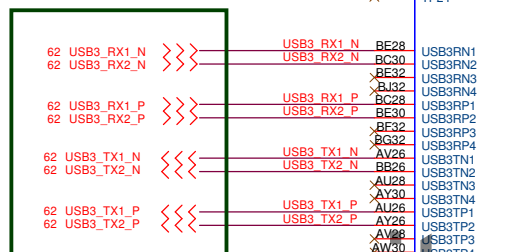
Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Layout Note:

Trace Length :
PCH ~~9000mil~~Cap~~1000mil~~CONN



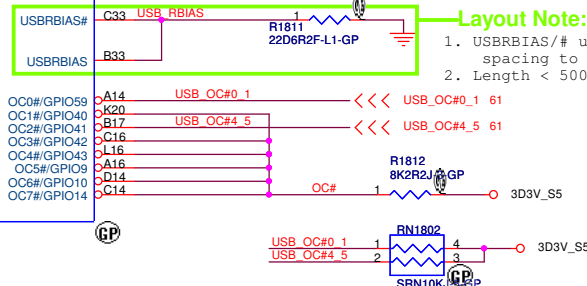
USB Table

Pair	Device
0	USB3.0 port2
1	USB3.0 port1, with Debug Port
2	USB2.0 port3
3	NC
4	NC
5	Touch Panel
6	HM76 NC
7	HM76 NC
8	NC
9	NC
10	Card reader
11	WLAN
12	NC
13	CAMERA

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Layout Note:

1. USBBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil



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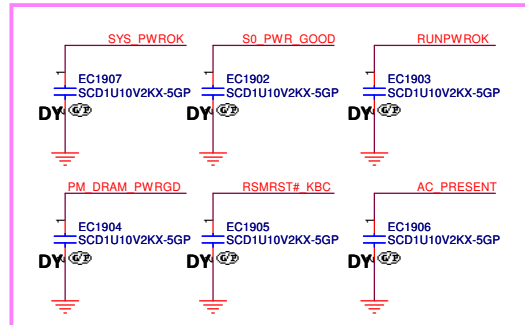
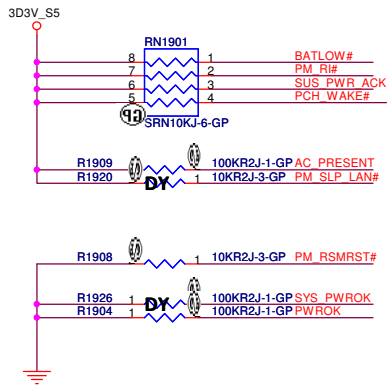
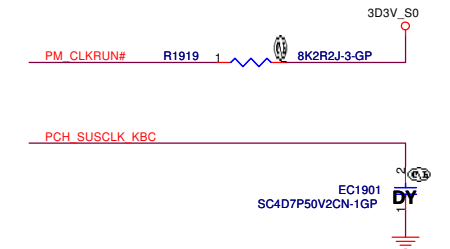
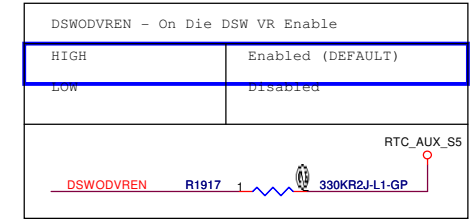
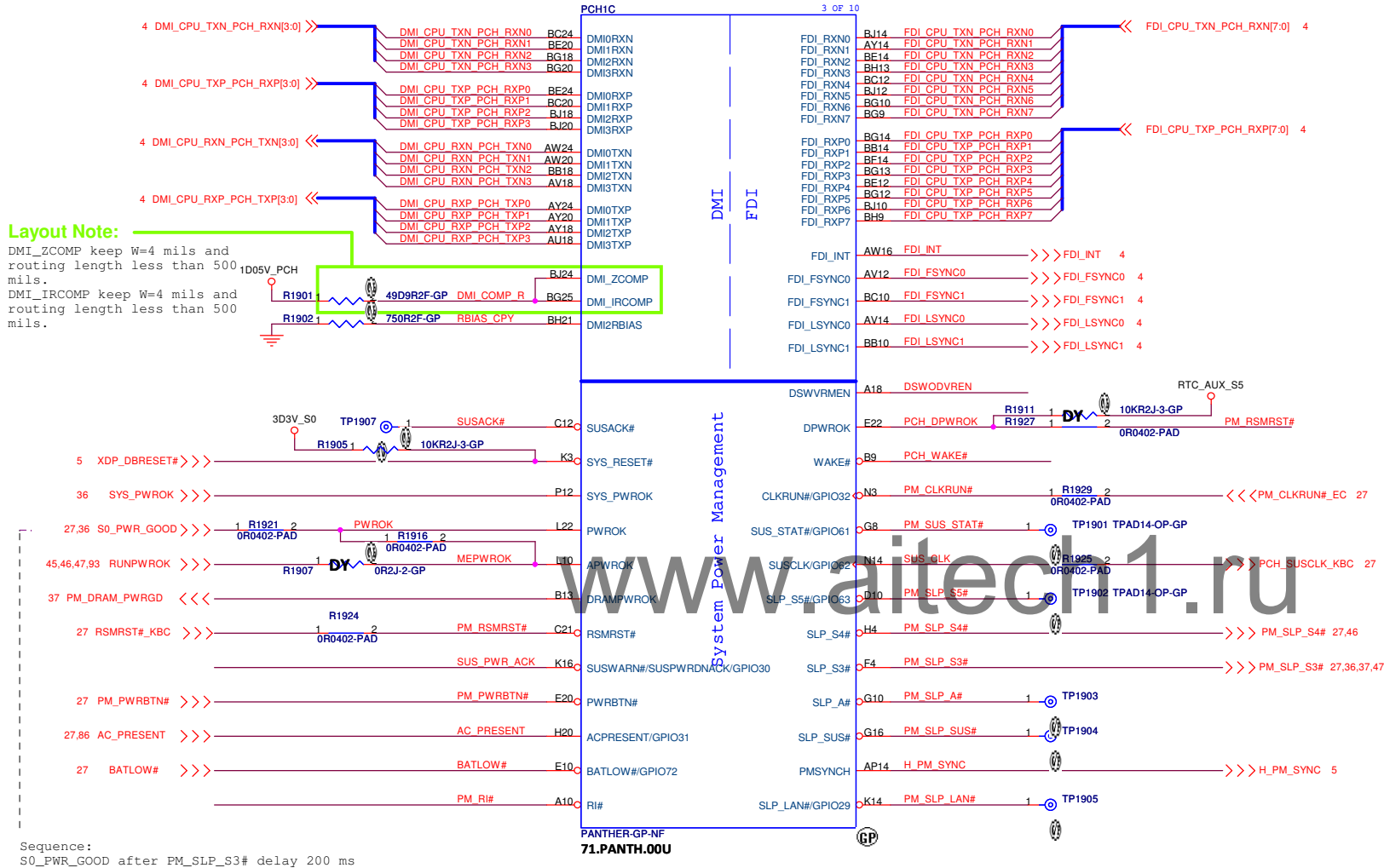
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Title			
PCH (PCI/USB/NVRAM)			
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	DNE40 14 CR DIS		
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SSID = PCH

Layout Note:

DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

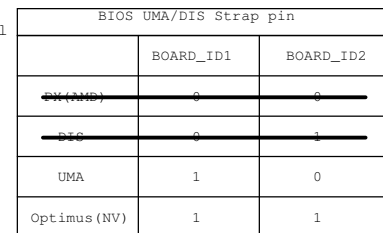
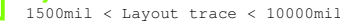


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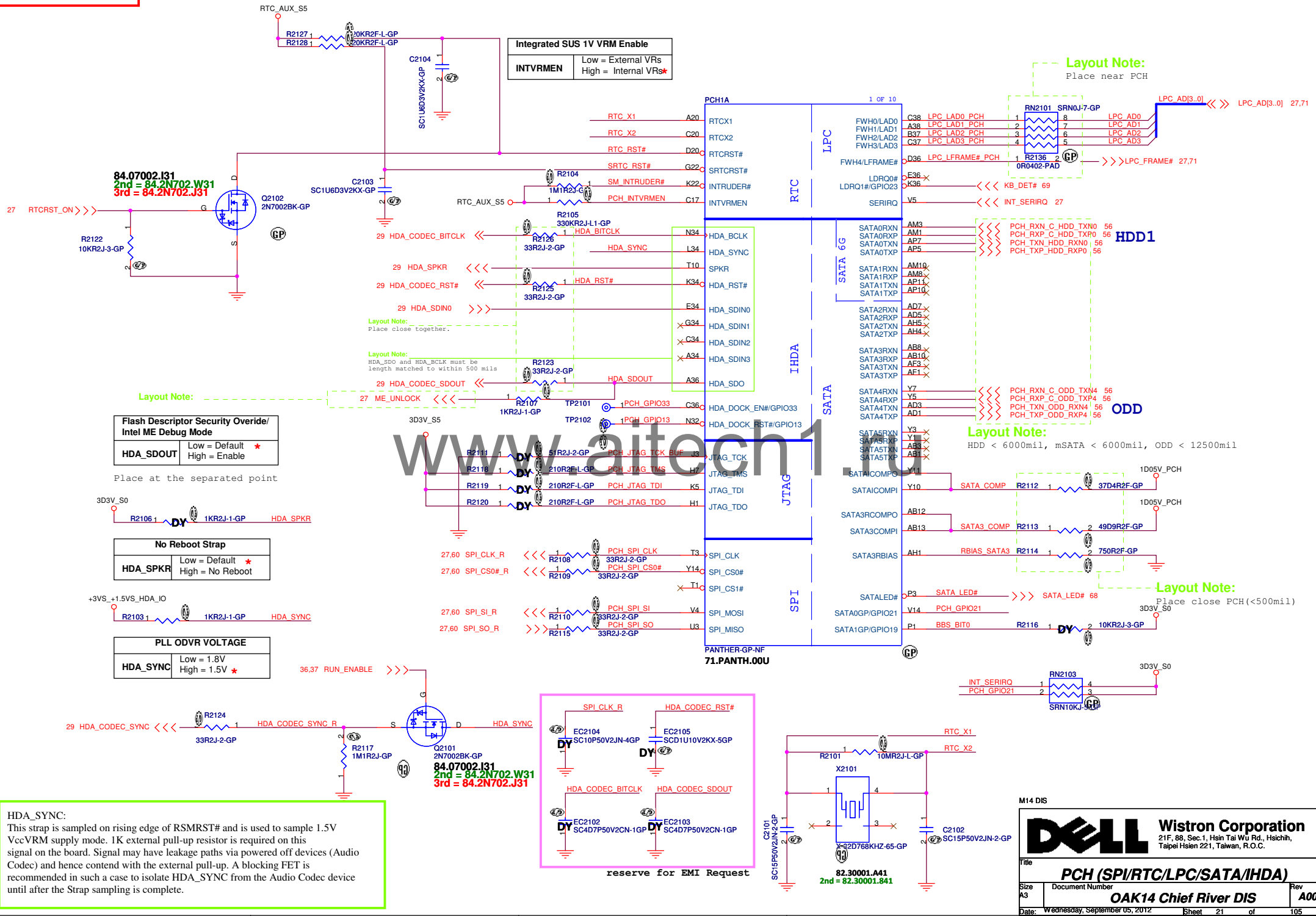


S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#



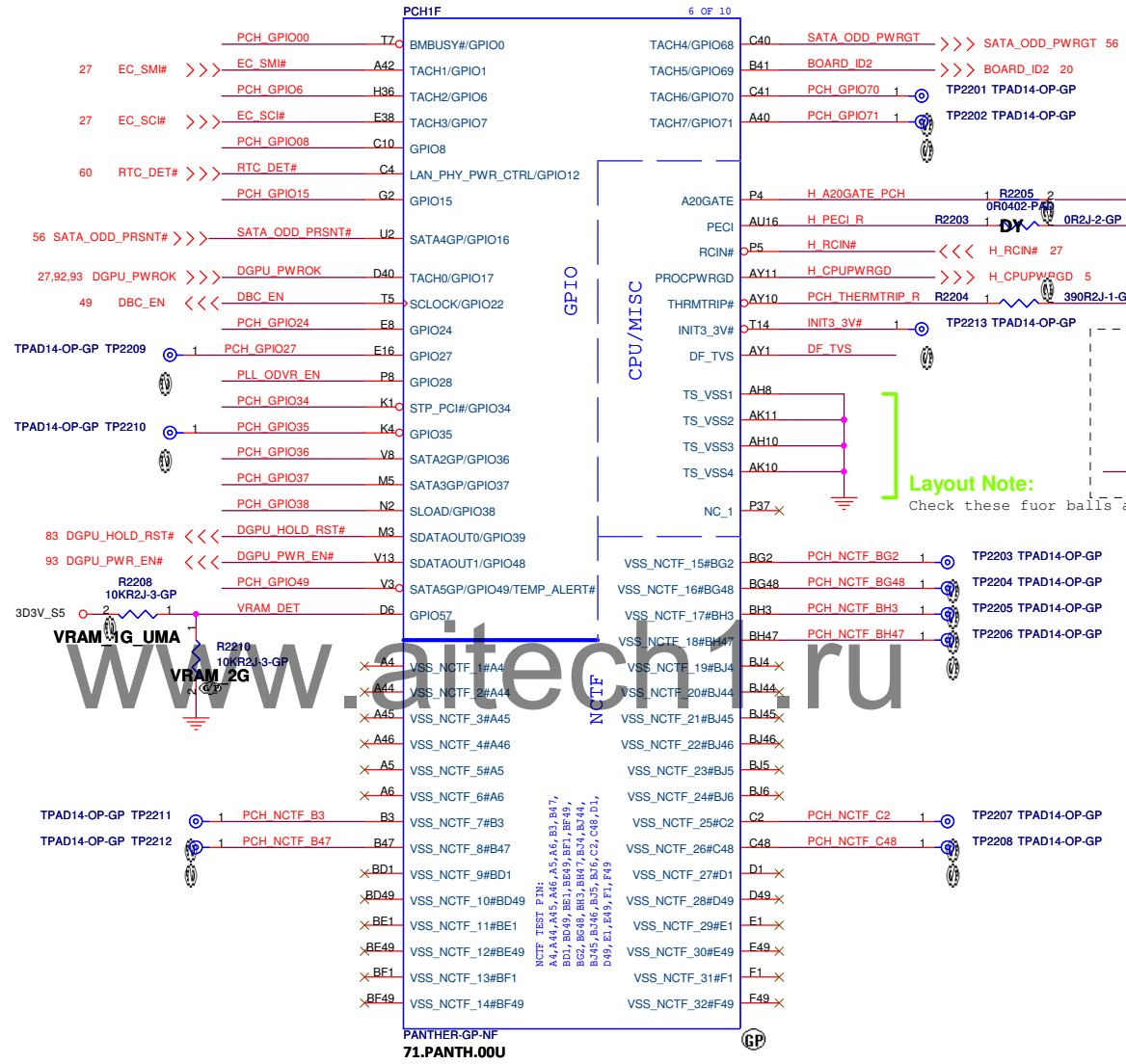
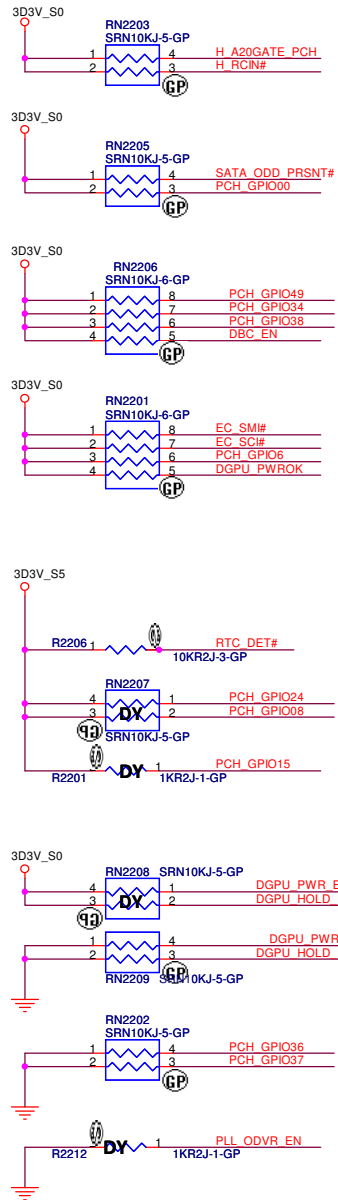
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SSID = PCH



HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

SSID = PCH



Layout Note:

Check these fuor balls are connected firstly, then to GND

PLL ON DIE VR ENABLE

GPIO28	weakly internal pull up 20k.
(PLL_ODVR_EN)	High - Enable
	LOW - Disable

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PCH (GPIO/CPU)

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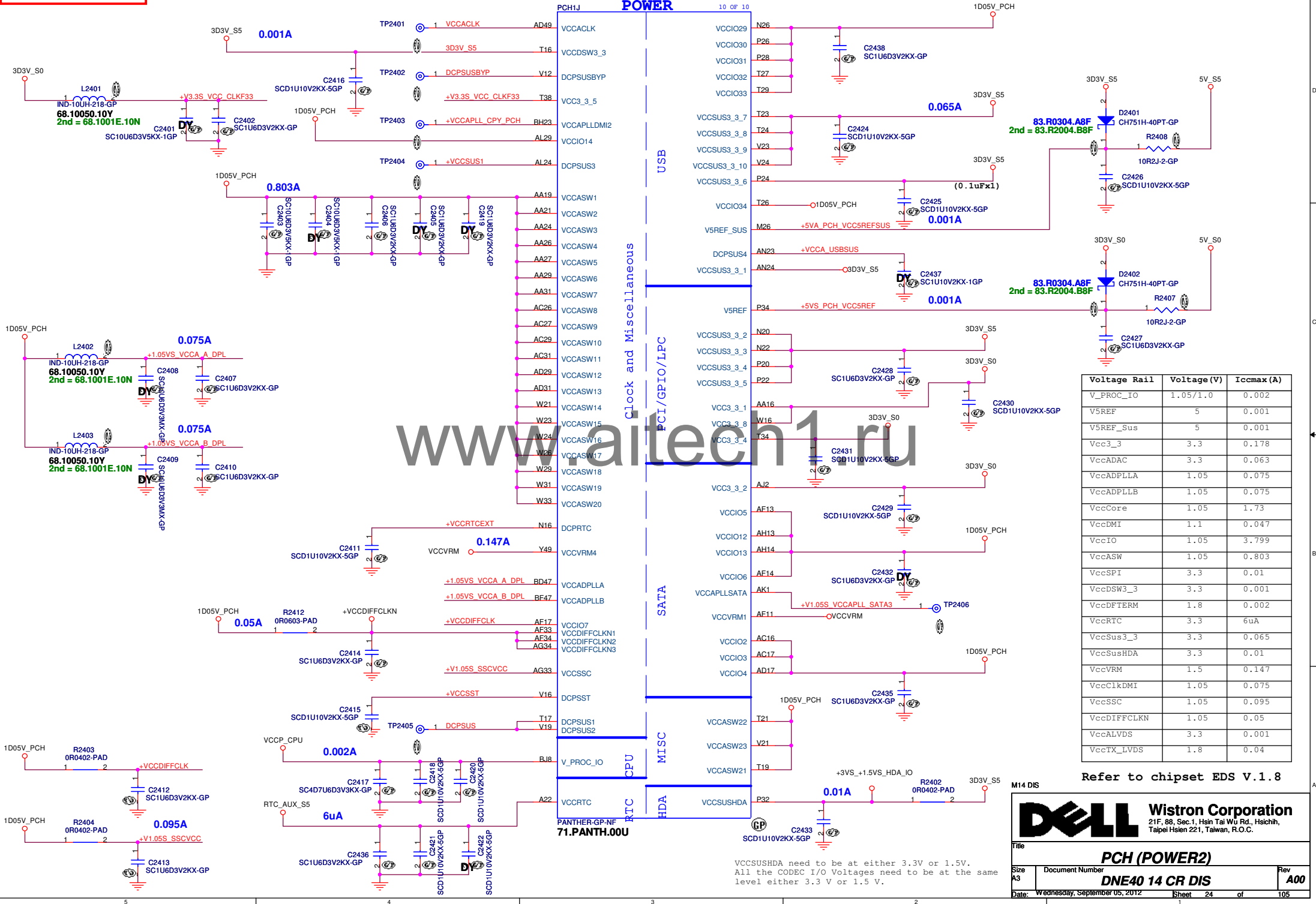
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SSID = PCH



SSID = PCH

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H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK9
AB11	VSS6	VSS85	AL16
AB14	VSS7	VSS86	AL17
AB39	VSS8	VSS87	AL19
AB4	VSS9	VSS88	AL2
AB43	VSS10	VSS89	AL21
AB5	VSS11	VSS90	AL23
AB7	VSS12	VSS91	AL26
AC19	VSS13	VSS92	AL27
AC2	VSS14	VSS93	AL31
AC21	VSS15	VSS94	AL33
AC24	VSS16	VSS95	AL34
AC33	VSS17	VSS96	AL48
AC34	VSS18	VSS97	AM11
AC48	VSS19	VSS98	AM14
AD10	VSS20	VSS99	AM36
AD11	VSS21	VSS100	AM39
AD12	VSS22	VSS101	AM43
AD13	VSS23	VSS102	AM45
AD19	VSS24	VSS103	AM46
AD24	VSS25	AM7	
AD26	VSS26	VSS104	AN2
AD27	VSS27	VSS105	AN29
AD33	VSS28	VSS106	AN3
AD34	VSS29	VSS107	AN31
AD36	VSS30	VSS108	AP12
AD37	VSS31	VSS109	AP19
AD38	VSS32	VSS110	AP28
AD39	VSS33	VSS111	AP30
AD4	VSS34	VSS112	AP32
AD40	VSS35	VSS113	AP38
AD42	VSS36	VSS114	AP4
AD43	VSS37	VSS115	AP42
AD45	VSS38	VSS116	AP46
AD46	VSS39	VSS117	AP8
AD8	VSS40	VSS118	AP8
AE2	VSS41	VSS119	AR2
AE3	VSS42	VSS120	AR48
AE10	VSS43	VSS121	AT11
AE12	VSS44	VSS122	AT13
AD14	VSS45	VSS123	AT18
AD16	VSS46	VSS124	AT22
AE16	VSS47	VSS125	AT26
AF19	VSS48	VSS126	AT28
AF24	VSS49	VSS127	AT30
AF26	VSS50	VSS128	AT32
AF27	VSS51	VSS129	AT34
AF29	VSS52	VSS130	AT39
AF31	VSS53	VSS131	AT42
AF38	VSS54	VSS132	AT46
AF4	VSS55	VSS133	AT7
AF42	VSS56	VSS134	AU24
AF46	VSS57	VSS135	AU30
AF5	VSS58	VSS136	AV16
AF7	VSS59	VSS137	AV20
AF8	VSS60	VSS138	AV24
AG19	VSS61	VSS139	AV30
AG2	VSS62	VSS140	AV38
AG31	VSS63	VSS141	AV4
AG48	VSS64	VSS142	AV43
AH11	VSS65	VSS143	AV8
AH3	VSS66	VSS144	AW14
AH36	VSS67	VSS145	AW18
AH39	VSS68	VSS146	AW2
AH40	VSS69	VSS147	AW22
AH42	VSS70	VSS148	AW26
AH46	VSS71	VSS149	AW28
AH7	VSS72	VSS150	AW34
AJ19	VSS73	VSS151	AW36
AJ21	VSS74	VSS152	AW40
AJ24	VSS75	VSS153	AW48
AJ33	VSS76	VSS154	AV11
AJ34	VSS77	VSS155	AY12
AK12	VSS78	VSS156	AY22
AK3	VSS79	VSS157	AY28
		VSS158	

PANTHER-GP-NF
71.PANTH.00U



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AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
B11	VSS162	VSS262	K39
B15	VSS163	VSS263	K46
B19	VSS164	VSS264	K7
B23	VSS165	VSS265	L18
B27	VSS166	VSS266	L2
B31	VSS167	VSS267	L20
B35	VSS168	VSS268	L26
B39	VSS169	VSS269	L28
B7	VSS170	VSS270	L36
F45	VSS171	VSS271	L48
BB12	VSS172	VSS272	M12
BB16	VSS173	VSS273	P16
BB20	VSS174	VSS274	M18
BB22	VSS175	VSS275	M22
BB24	VSS176	VSS276	M24
BB28	VSS177	VSS277	M30
BB30	VSS178	VSS278	M32
BB38	VSS179	VSS279	M34
BB4	VSS180	VSS280	M38
BB46	VSS181	VSS281	M4
BC14	VSS182	VSS282	M42
BC18	VSS183	VSS283	M46
BC2	VSS184	VSS284	M8
BC22	VSS185	VSS285	N18
BC26	VSS186	VSS286	P30
BC32	VSS187	VSS287	N47
BC34	VSS188	VSS288	P11
BC36	VSS189	VSS289	P18
BC40	VSS190	VSS290	T33
BC42	VSS191	VSS291	P40
BC48	VSS192	VSS292	P43
BD46	VSS193	VSS293	P47
BD5	VSS194	VSS294	P7
BE22	VSS195	VSS295	R2
BE26	VSS196	VSS296	R48
BE40	VSS197	VSS297	T12
BF10	VSS198	VSS298	T31
BF12	VSS199	VSS299	T37
BF16	VSS200	VSS300	T4
BF20	VSS201	VSS301	W34
BF22	VSS202	VSS302	T46
BF24	VSS203	VSS303	T47
BF26	VSS204	VSS304	T8
BF28	VSS205	VSS305	V11
BF3	VSS206	VSS306	V17
BF36	VSS207	VSS307	V26
BF40	VSS208	VSS308	V27
BF42	VSS209	VSS309	V29
BF46	VSS210	VSS310	V31
BG17	VSS211	VSS311	V36
BG24	VSS212	VSS312	V39
BG33	VSS213	VSS313	V43
BG44	VSS214	VSS314	V7
BG8	VSS215	VSS315	W17
BH11	VSS216	VSS316	W19
BH15	VSS217	VSS317	W2
BH17	VSS218	VSS318	W27
BH19	VSS219	VSS319	W48
H10	VSS220	VSS320	Y12
BH27	VSS221	VSS321	Y38
BH31	VSS222	VSS322	Y4
BH33	VSS223	VSS323	Y42
BH35	VSS224	VSS324	Y46
BH39	VSS225	VSS325	Y8
BH43	VSS226	VSS326	BG29
BH7	VSS227	VSS327	N24
D3	VSS228	VSS328	AJ3
D12	VSS229	VSS329	AD47
D16	VSS230	VSS330	B43
D18	VSS231	VSS331	BE10
D22	VSS232	VSS332	BG41
D24	VSS233	VSS333	G14
D26	VSS234	VSS334	H16
D30	VSS235	VSS335	T36
D32	VSS236	VSS336	BG22
D34	VSS237	VSS337	BG24
D38	VSS238	VSS338	C22
D42	VSS239	VSS339	AP13
D46	VSS240	VSS340	M14
E18	VSS241	VSS341	AP3
E26	VSS242	VSS342	AP1
G18	VSS243	VSS343	BE16
G20	VSS244	VSS344	BC16
G26	VSS245	VSS345	BG28
G28	VSS246	VSS346	VSS351
G36	VSS247	VSS347	VSS352
G48	VSS248	VSS348	BJ28
H12	VSS249	VSS349	
H18	VSS250	VSS350	
H22	VSS251	VSS351	
H24	VSS252	VSS352	
H26	VSS253		
H30	VSS254		
H32	VSS255		
H34	VSS256		
F3	VSS257		
	VSS258		

PANTHER-GP-NF
71.PANTH.00U



M14 DIS



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Title			PCH (VSS)
Size	Document Number	Rev	
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Taipei Hsien 221, Taiwan, R.O.C.

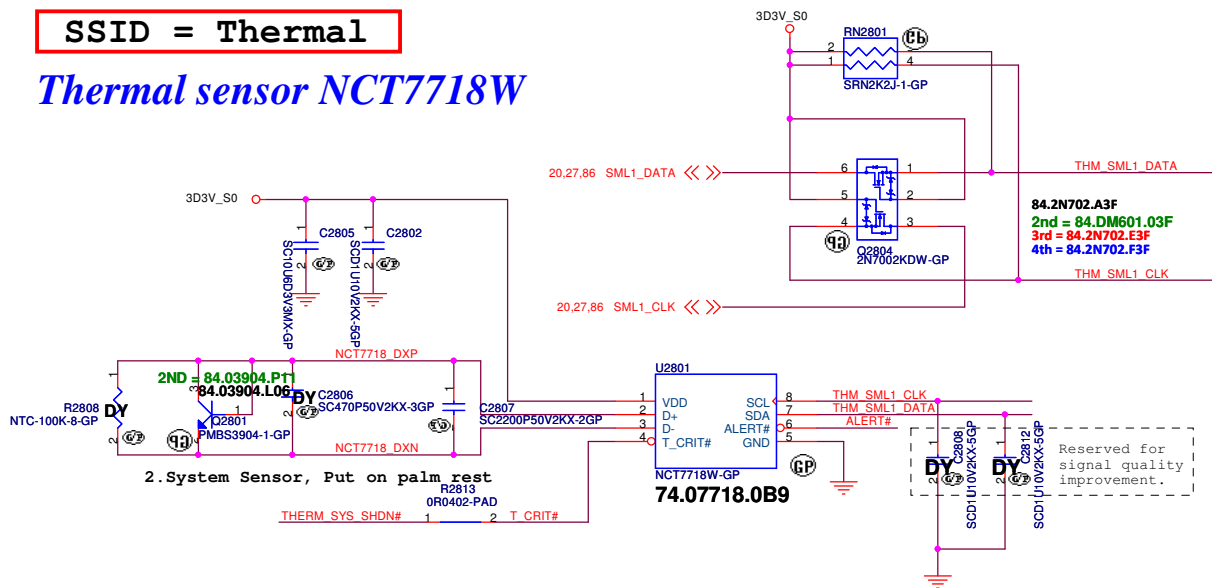
Title

Reserved

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SSID = Thermal

Thermal sensor NCT7718W

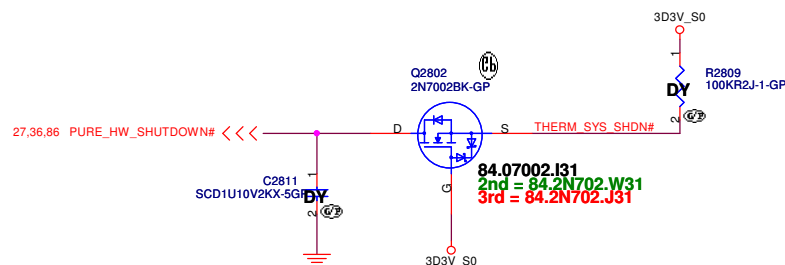


ALERT# /T CRIT#
Pull-up Resistor

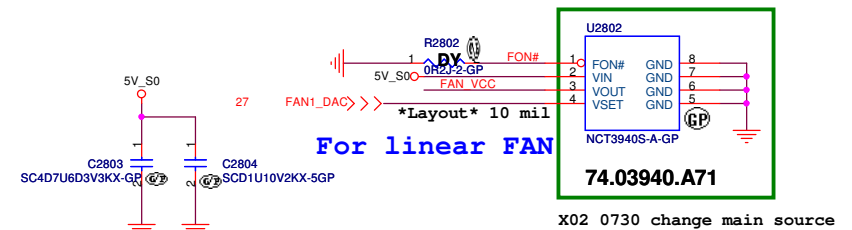
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing. and route has to be away from the high noise area.
Put the C2807 2200pF to close the NCT7718W

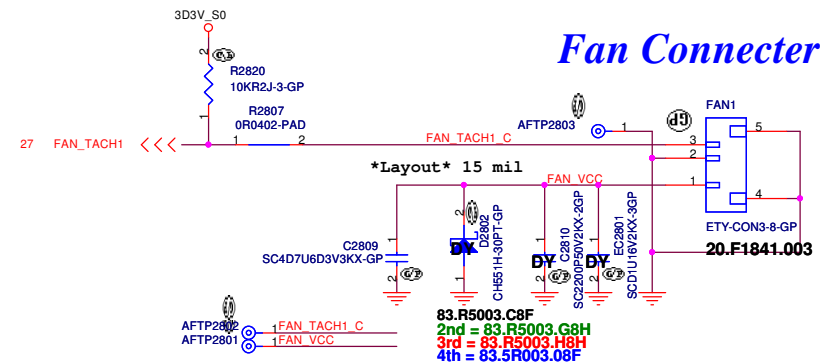


Fan controller NCT3940S-A



X02 0730 change main source

Fan Connector



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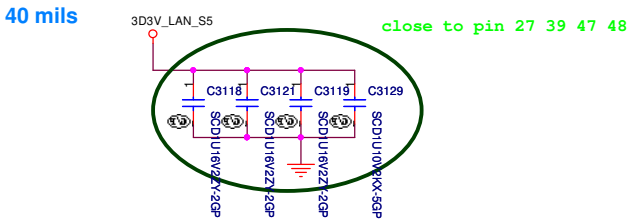
Title

Reserved

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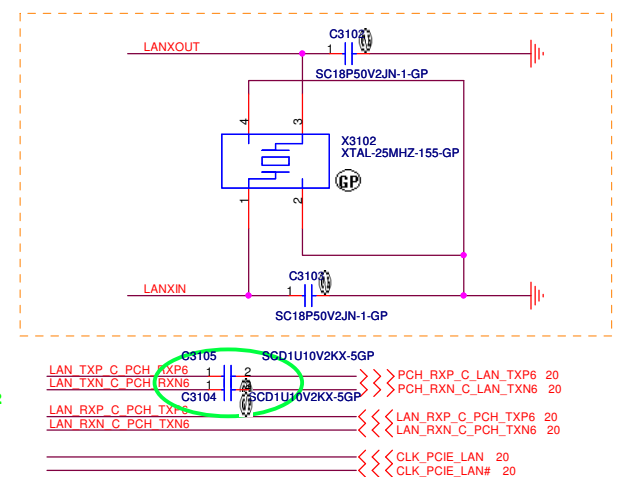
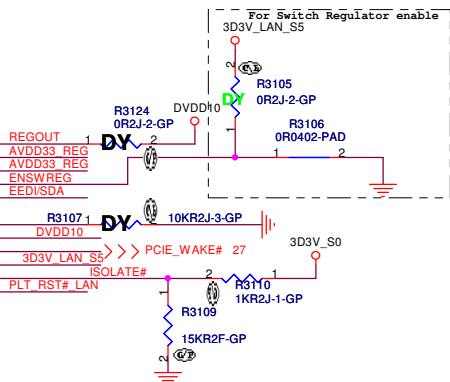
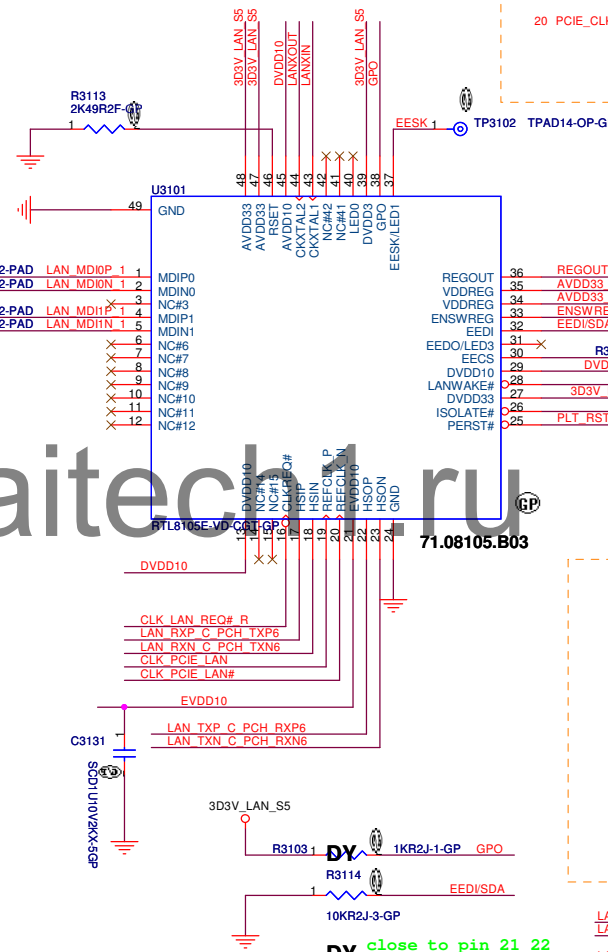
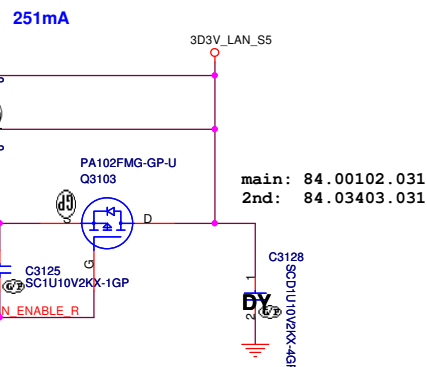
71.08105E.B0



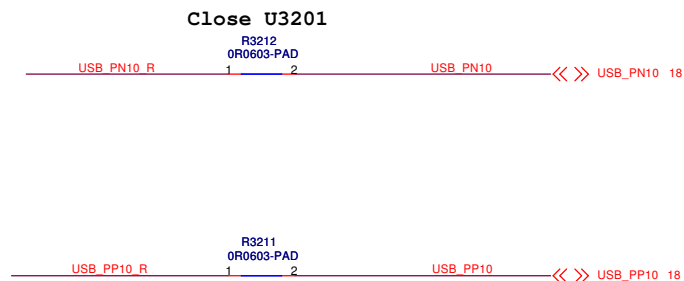
5,18,27,65,71,83 PLT_RST# >>>

Q3104
PMBS3904-1-GP
R3123

OR0402-PAD



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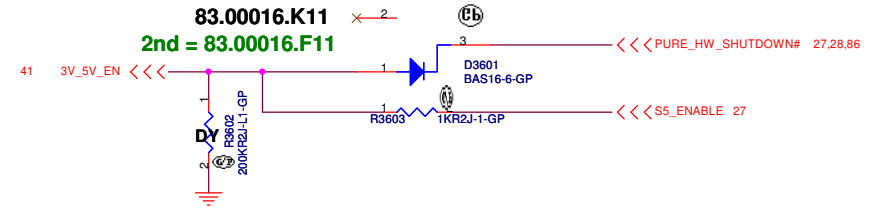
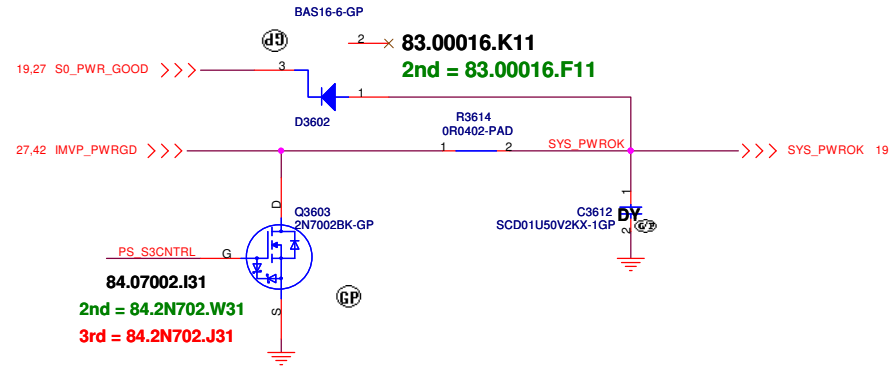
Title

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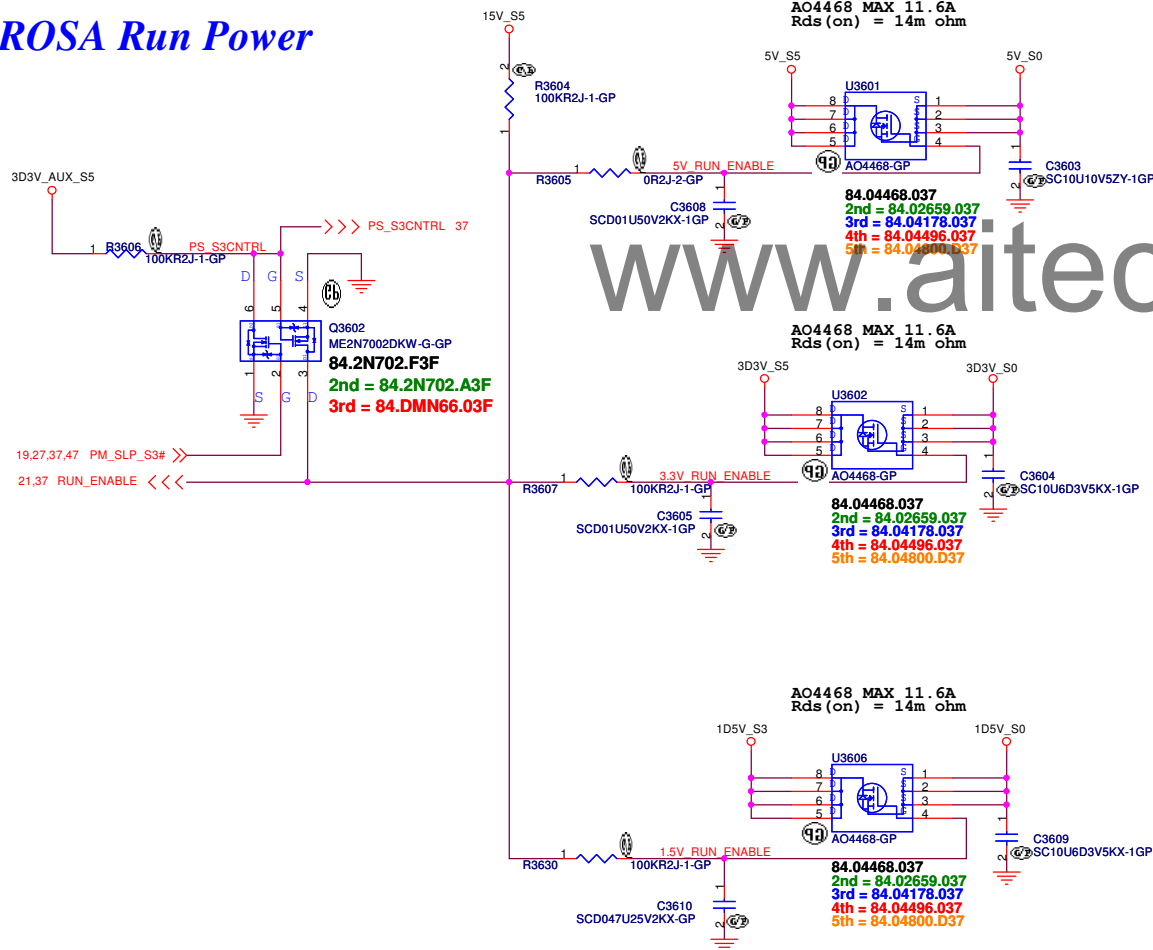
Size	Document Number	Rev
A3	OAK14 Chief River DIS	A00

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SSID = Reset.Suspend



ROSA Run Power



5V_S0

+5V_RUN Consumption
Peak current ?A
Design current ?A

3D3V_S0

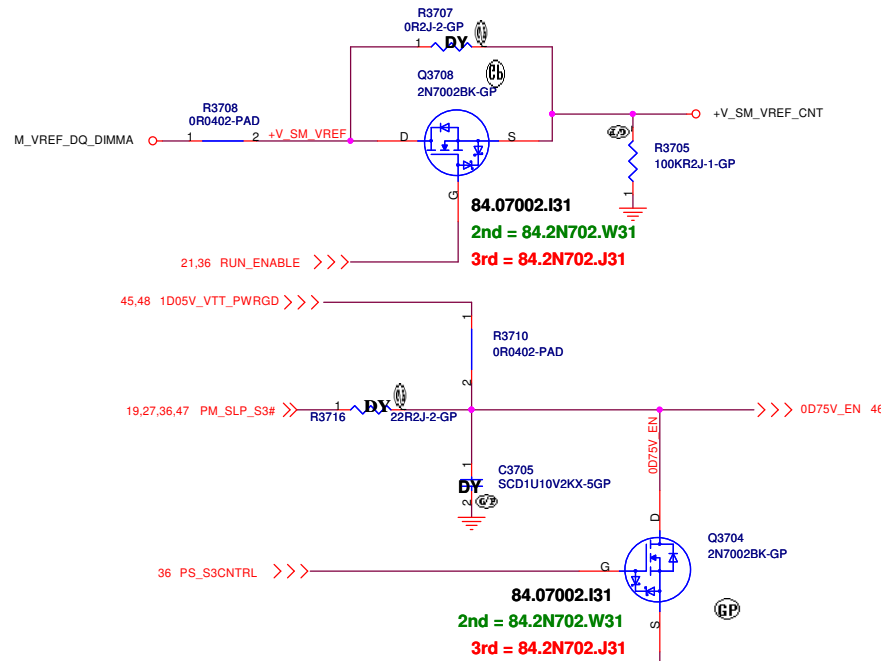
+3.3V_RUN Consumption
Peak current ?A
Design current ?A

1D5V_S0

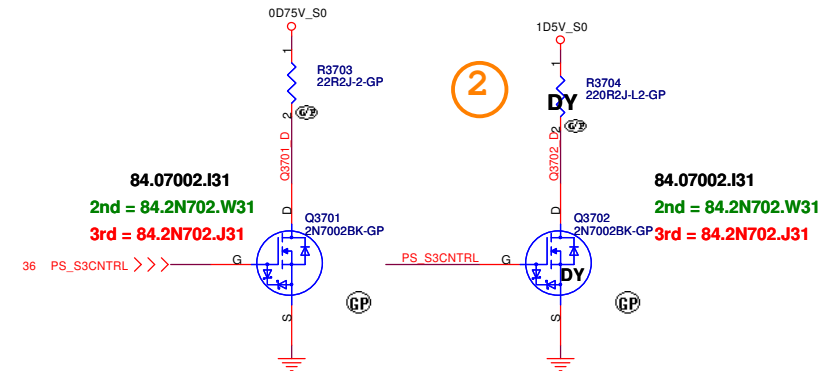
+1.5V_RUN Consumption
Peak current ?A
Design current ?A

M14 DIS

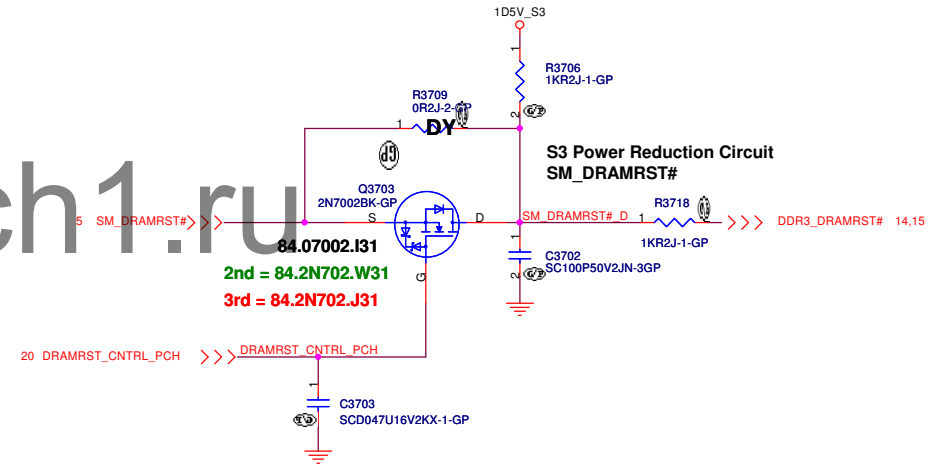
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



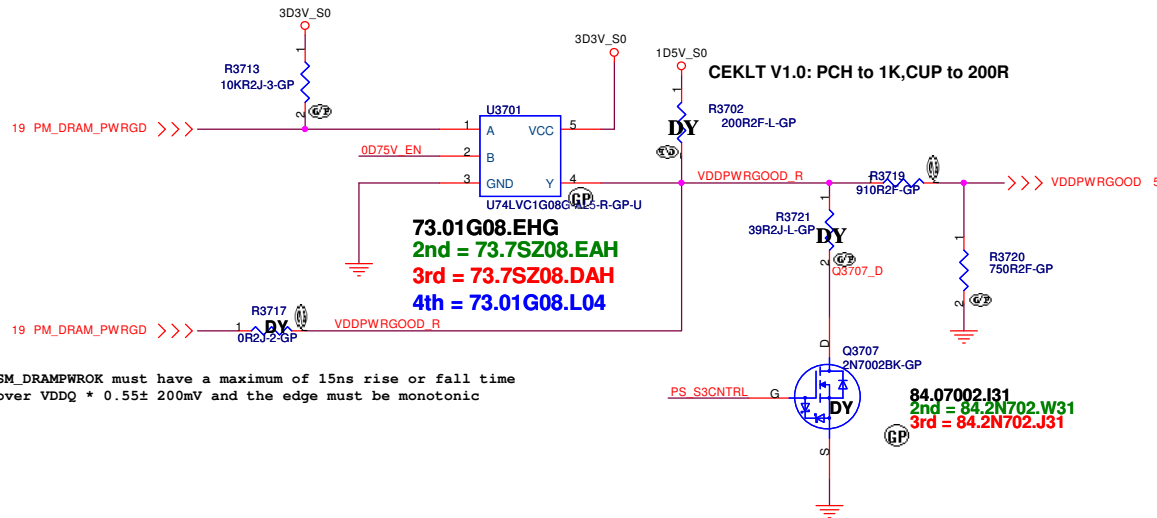
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

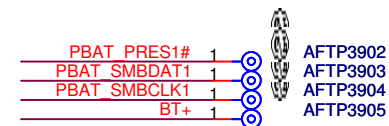
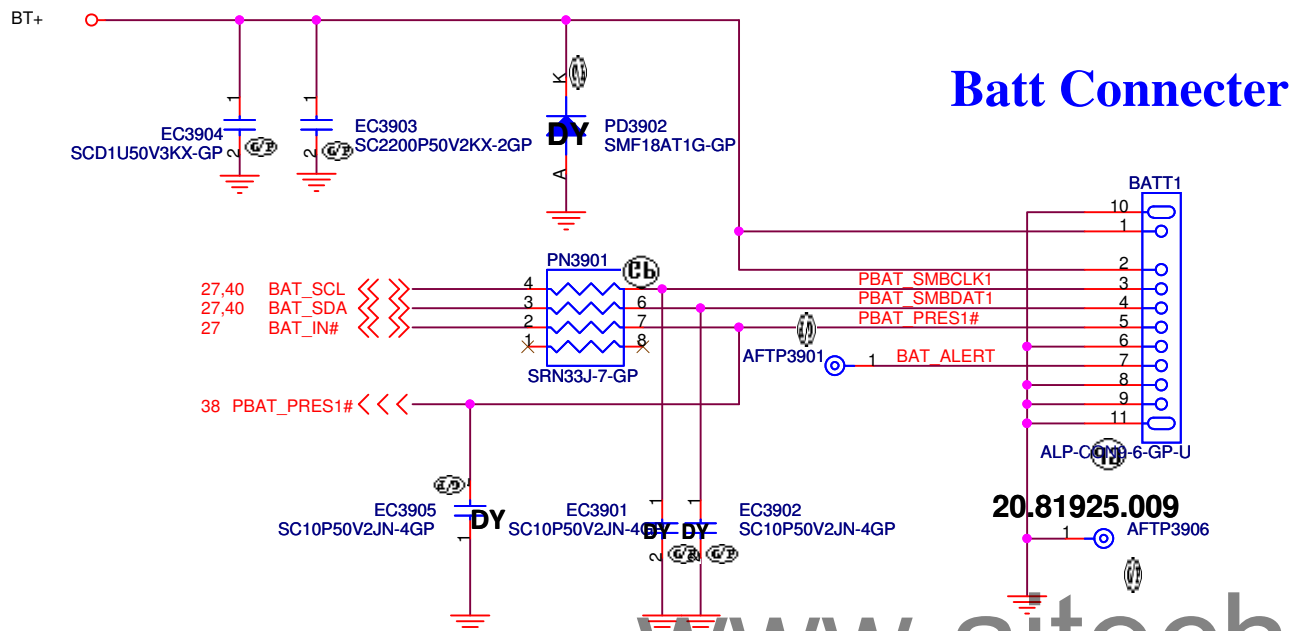
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M14 DIS

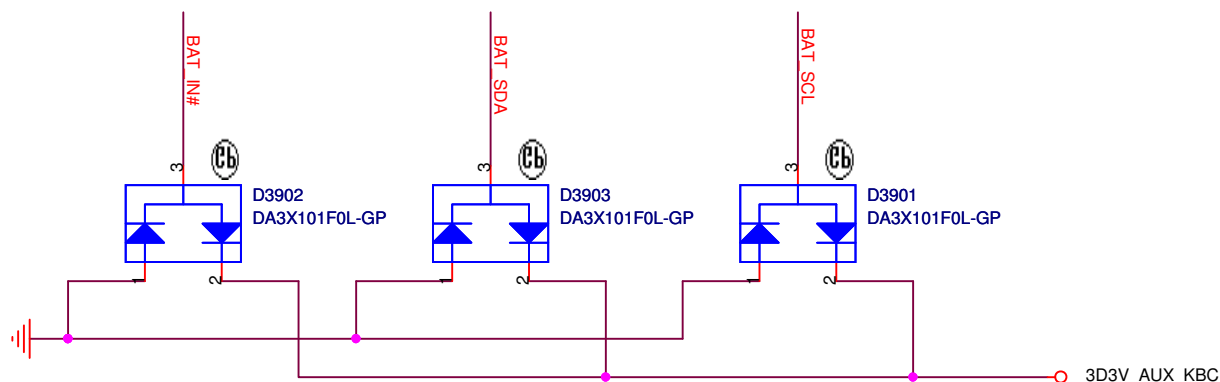
Layout Note:
PSID Layout width > 25mil



SSID = PWR.Support



Placement: Close to Batt Connector



83.3X101.011

2nd = 83.BAV99.H11

3rd = 83.00099.M11

83.3X101.011

2nd = 83.BAV99.H11

3rd = 83.00099.M11

83.3X101.011

2nd = 83.BAV99.H11

3rd = 83.00099.M11

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BATT CONN

Size
A4

Document Number

OAK14 Chief River DIS

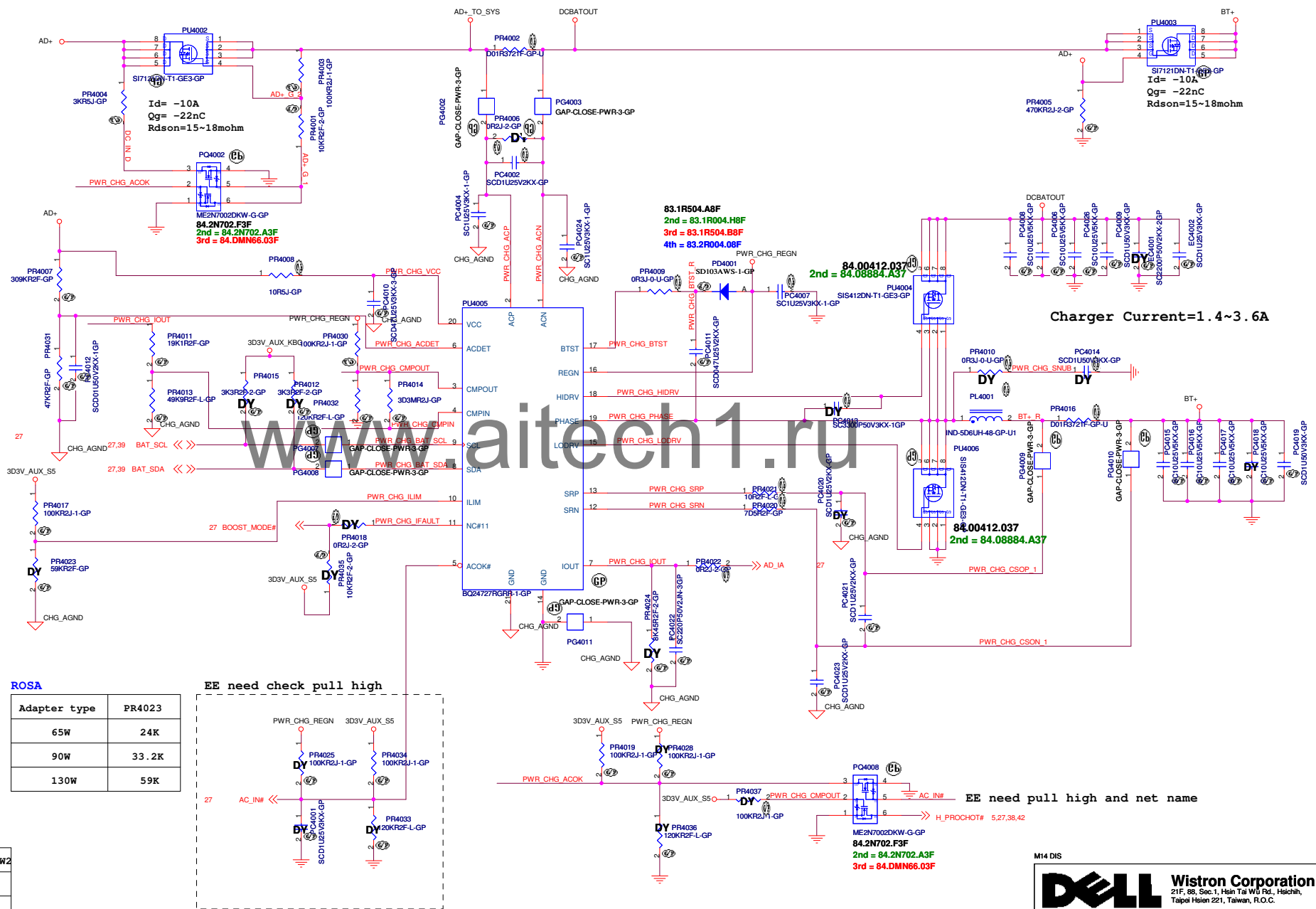
Rev
A00

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EC code only BQ24707

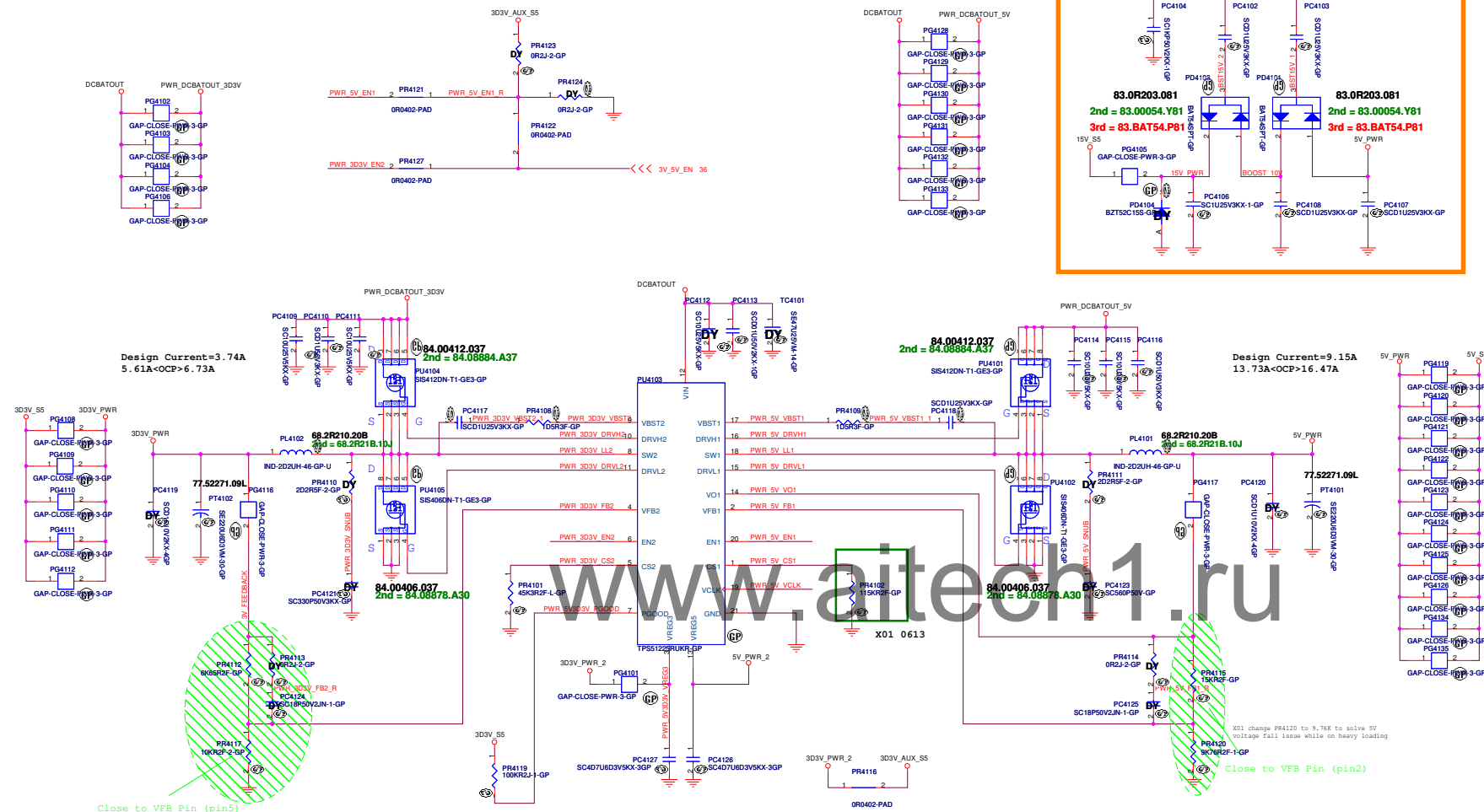
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1



M14 DIS

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		CHARGER BQ24727	
Size	Document Number		Rev
	DNE40 14 CR DIS		A00
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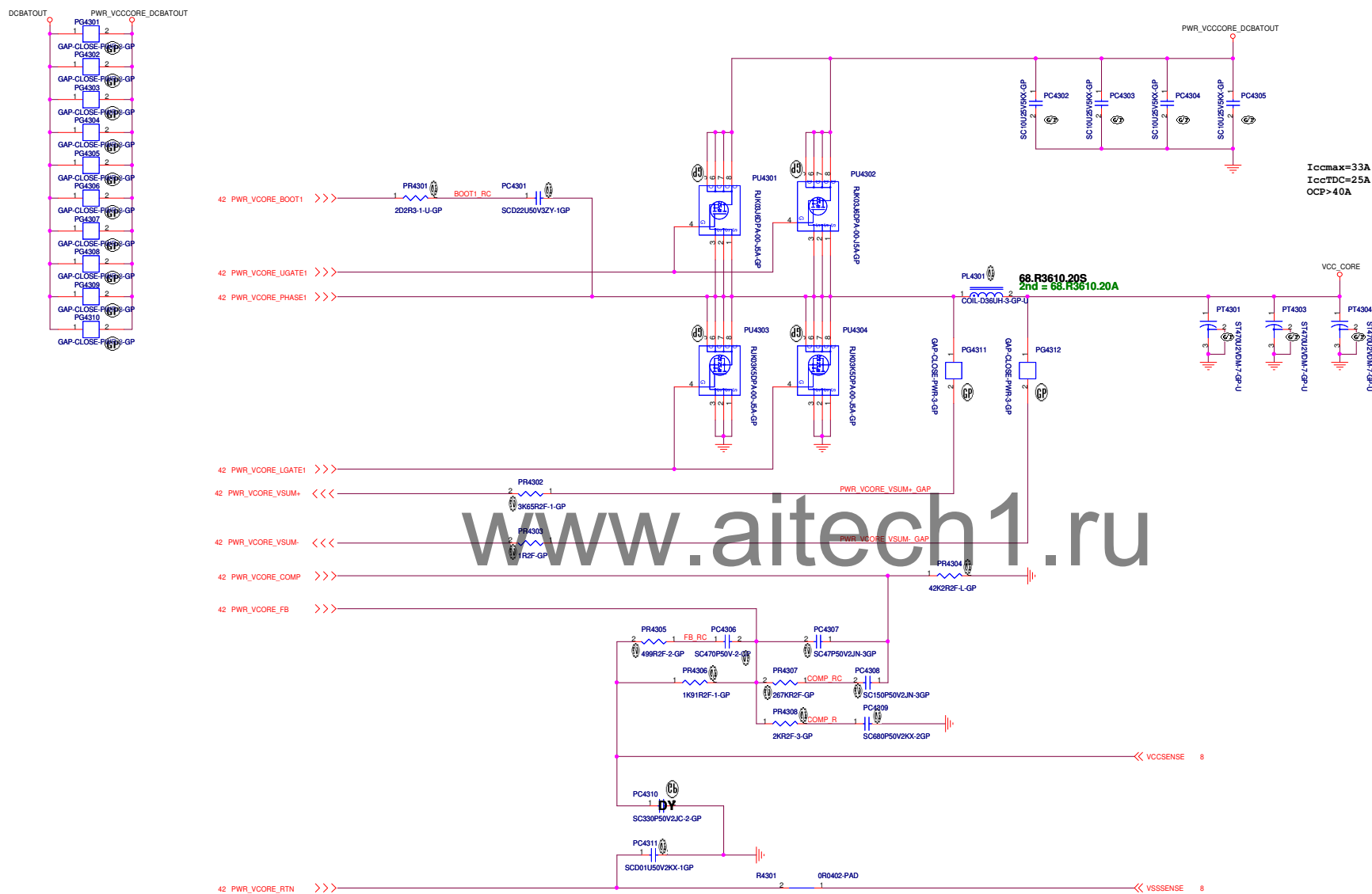
```
SSID = PWR.Plane.Regulator_5v3p3v
```



I/P cap: CHIP CAP C 100 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCCM063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsui/ 17mohm / 77.52271.09L
H/S: SIS412DN-T1-GE3 / 24mOhm/30mohm/4.5Vgs / 84.00412.037
L/S: SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm/4.5Vgs / 84.00406.037

```
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND N 3.3UH PCCM0623T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsui/ 17mohm / 77.52271.09L
H/S:S1S412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:S1S406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037
```


SSID = CPU.Regulator



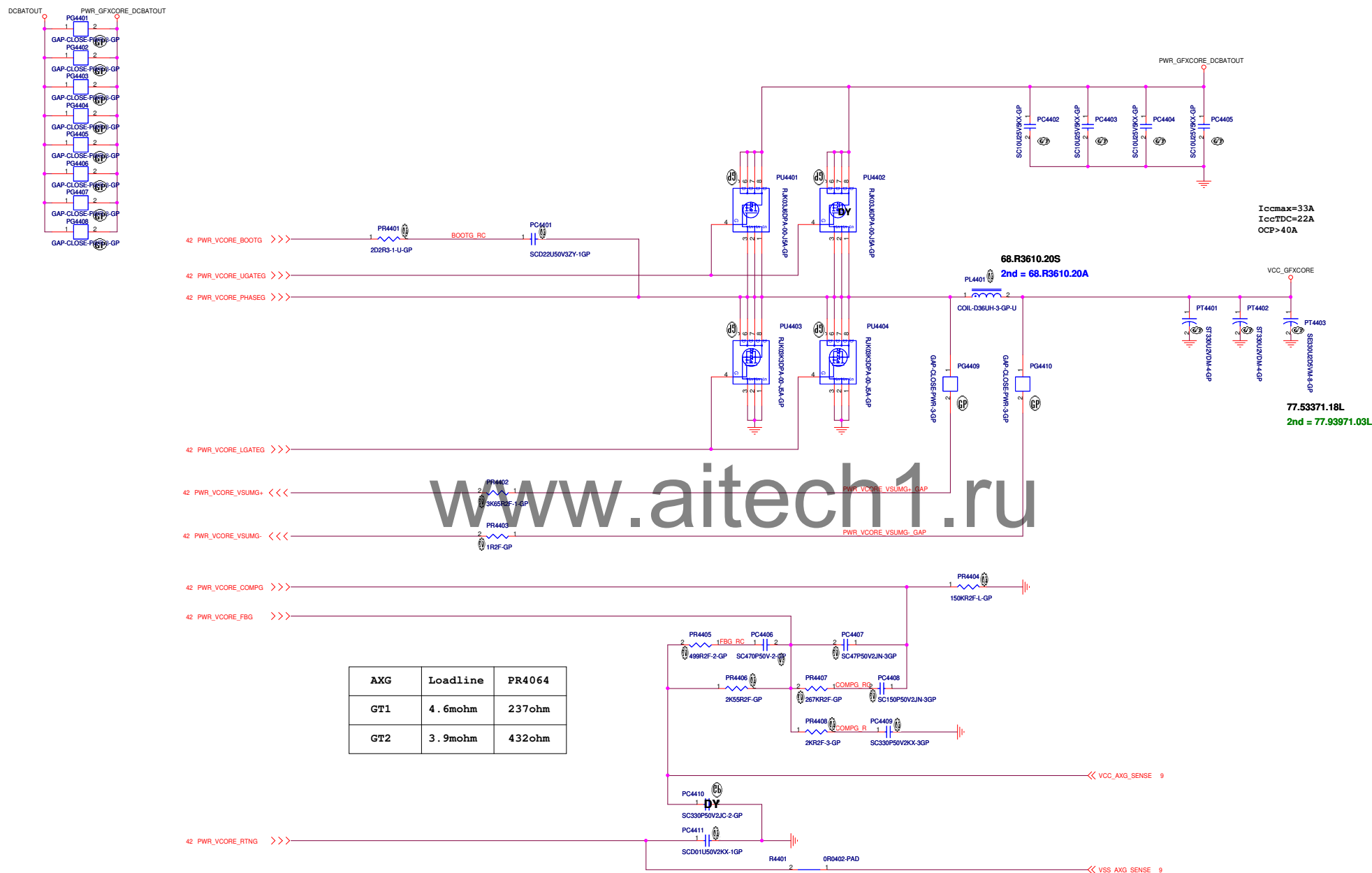
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP EL 470U 2V 7.3*4.3 ESR=0.0045 3.8Arms Panasonic/79.47719.9BL
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K5DPA-00#J5A / 3mohm/3.9mOhm@4.5Vgs/ 84.00035.037

M14 DIS

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File
ISL95833 CPU CORE(2/3)
Size C Document Number OAK14 Chief River DIS Rev A00
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```
SSID = CPU.Regulator
```

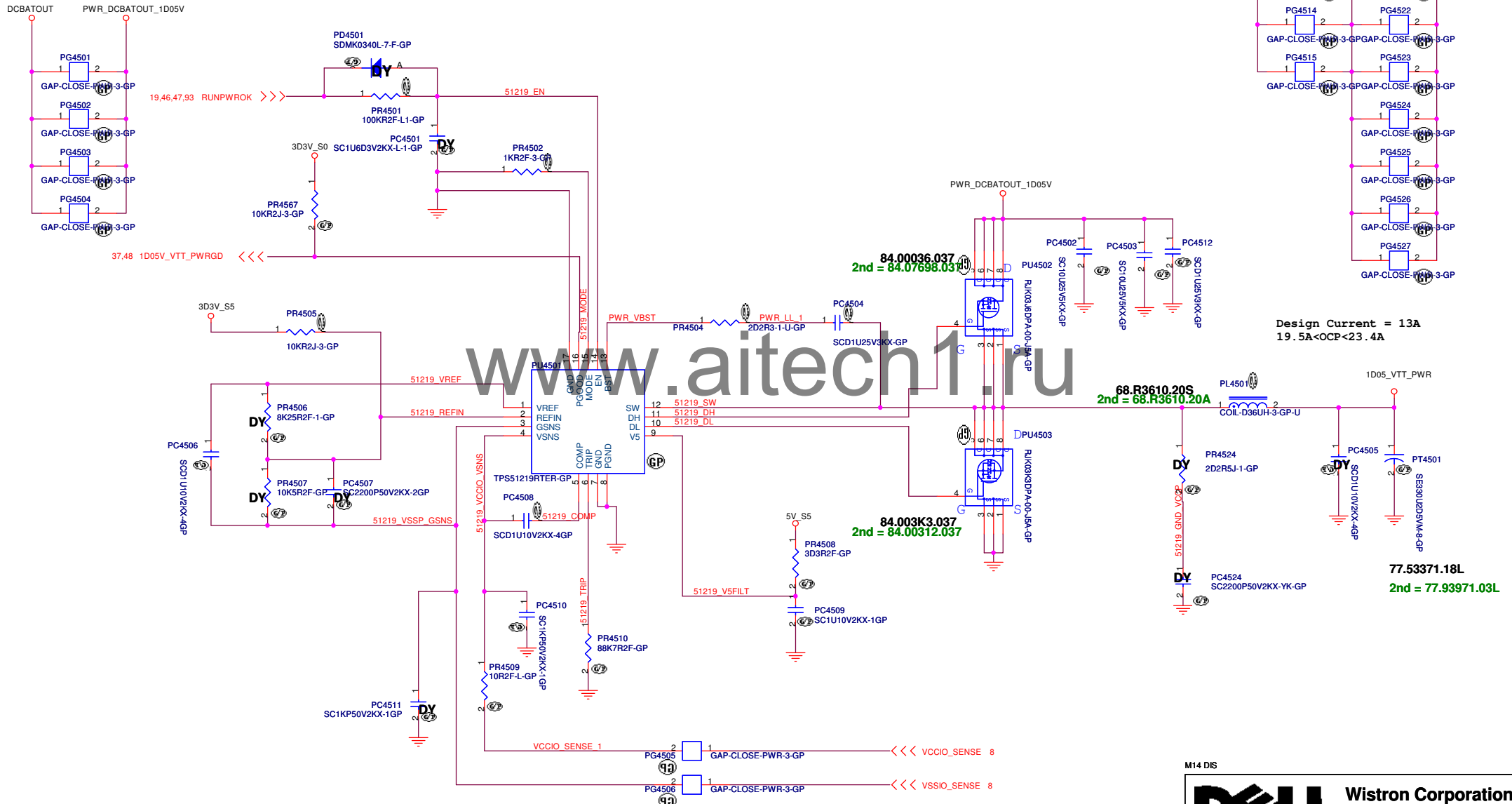


AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP 330U 2V EEPF030331XE 3.5Arms Panasonic/79.33719.20L
H/S: RJK03K36DPA-00#J5A / 10mohm/13mohm@4.5Vgs/ 84.00036.037
L/S: RJK03K36DPA-00#J5A / 4.9mohm/6.1mohm@4.5Vgs/ 84.00033.037

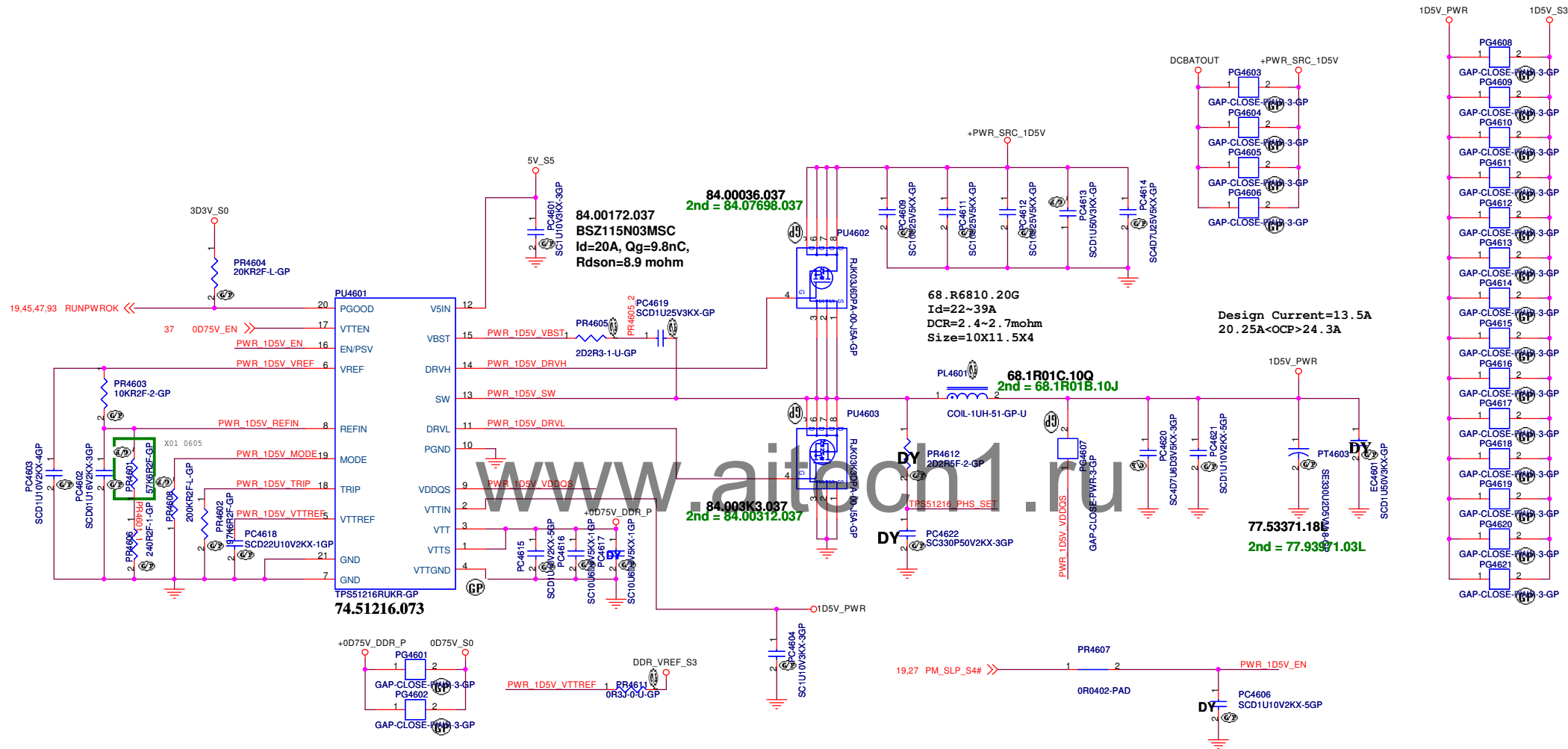
SSID = PWR.Plane.Regulator_1p05v_pch/vccp_cpu

TPS51219 for 1D05V_VTT



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHK 0.36UH PCMC104T-R36MH 1.05mohm/ Isat =60A rms68.R3610.20S
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOK 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S: RJK03J6DPA-00#J5A / 10mohm/13mOhm@4.5Vgs/ 84.00036.037
 L/S: RJK03K3DPA-00#J5A / 4.9mohm/6.1mOhm@4.5Vgs/ 84.003K3.037

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Title

TPS51216 +1.5V SUS

Size A3

Document Number

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Date: Wednesday, September 05, 2012

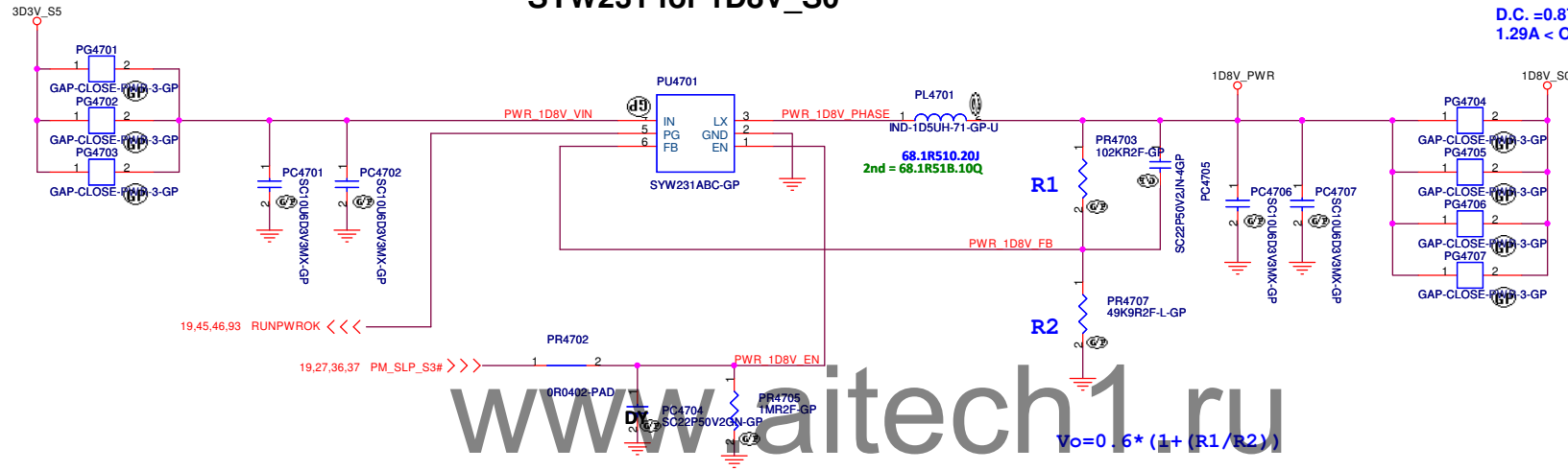
Rev

A00

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SYW231 for 1D8V_S0

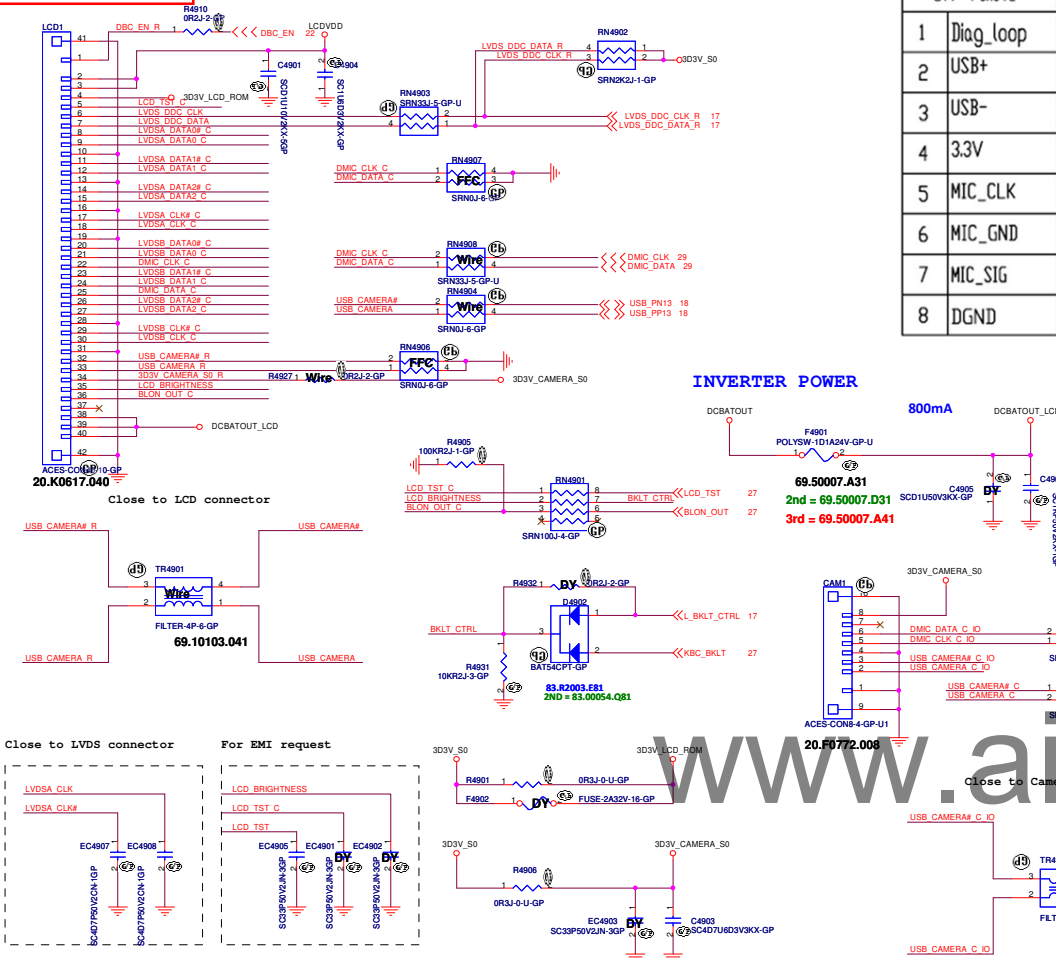
D.C. =0.87A
1.29A < OCP <1.52A



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DELL		Wistron Corporation	
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Title SYW231 1D8V S0			
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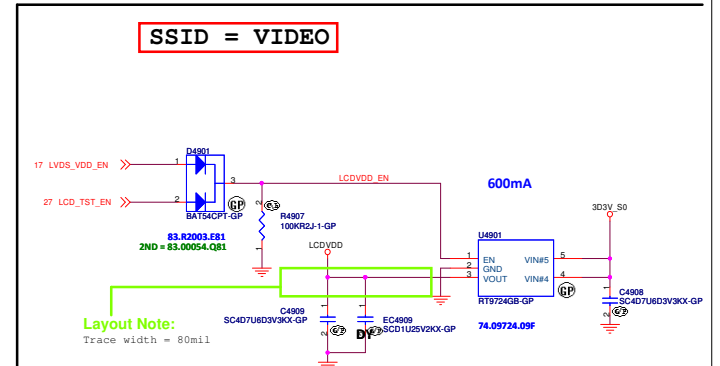
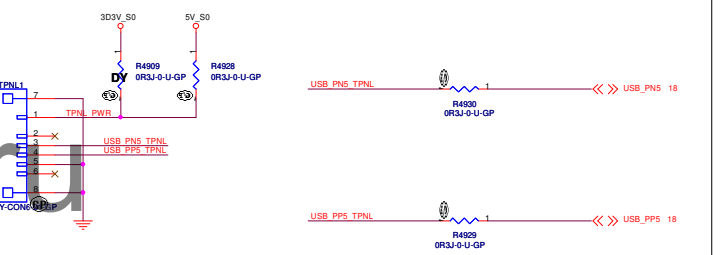
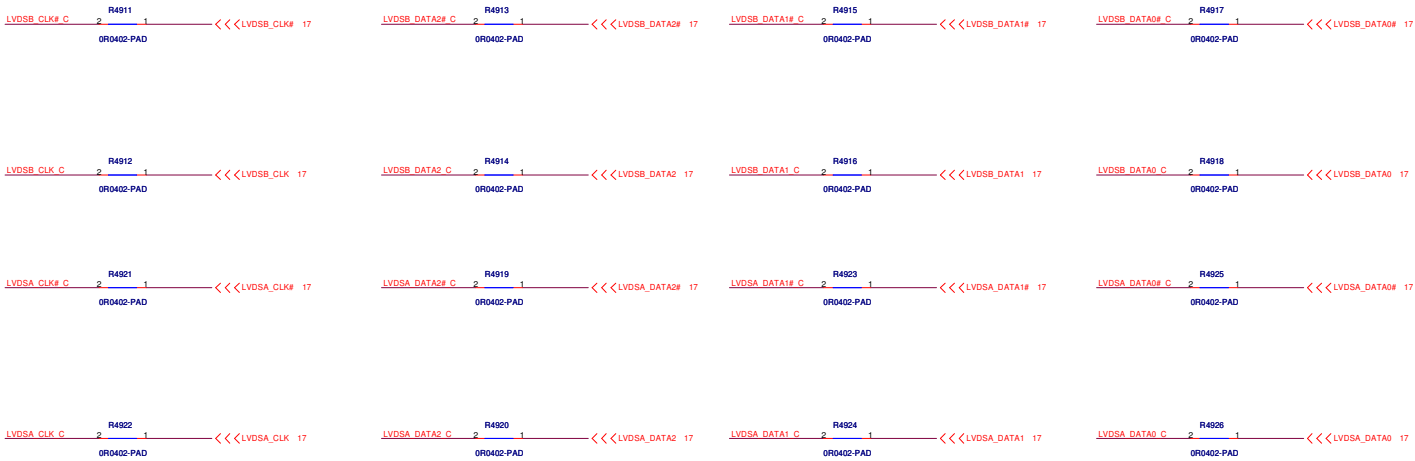
SSID = VIDEO



CN Table	
1	Diag_loop
2	USB+
3	USB-
4	3.3V
5	MIC_CLK
6	MIC_GND
7	MIC_SIG
8	DGND

MB Connector	是否接線	Wire (40 PIN)	Pin 10 (GND 實體線)
Pin 10	GND	Y	Pin 10 GND
Pin 13	GND	Y	Pin 13 GND
Pin 16	GND	Y	Pin 16 GND
Pin 19	GND	Y	Pin 19 GND
Pin 22	GND	Y	Pin 22 GND
Pin 25	GND	Y	Pin 22 GND
Pin 28	GND	Y	Pin 28 GND
Pin 31	GND	Y	Pin 31 GND
Pin 32	GND	Y	Pin 32 GND
Pin 33	GND	Y	Pin 33 GND
Pin 34	3D3V_CAMERA_S0	Y	NC(0 ohm DY)

PIN	MB Connector	是否接線	PIN	Camera Module Conn
1	DGND	Y	8	DGND
2	USB_CAMERA_C (USB+)	Y	2	USB_CAMERA_C (USB+)
3	USB_CAMERA#_C (USB-)	Y	3	USB_CAMERA#_C (USB-)
4	DMIC_GND	Y	6	DMIC_GND
5	DMIC_CLK_C	Y	5	DMIC_CLK_C
6	DMIC_DATA_C	Y	7	DMIC_DATA_C
7	NC	N	1	NC
8	3D3V_CAMERA_S0	Y	4	3D3V_CAMERA_S0



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Title

CRT Connector

Size
A3

Document Number
OAK14 Chief River DIS

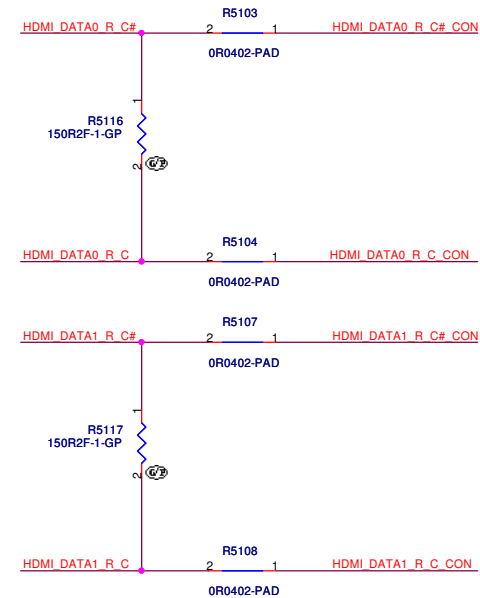
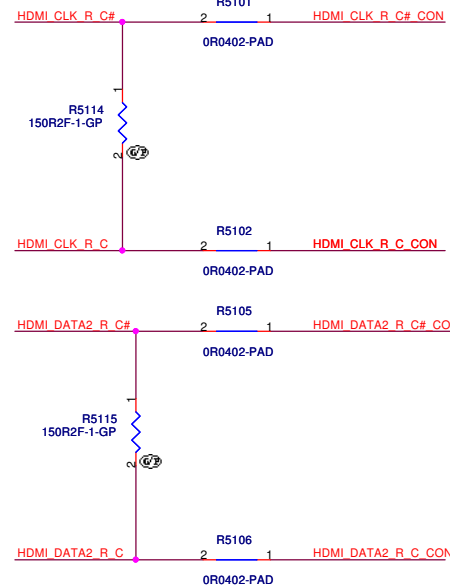
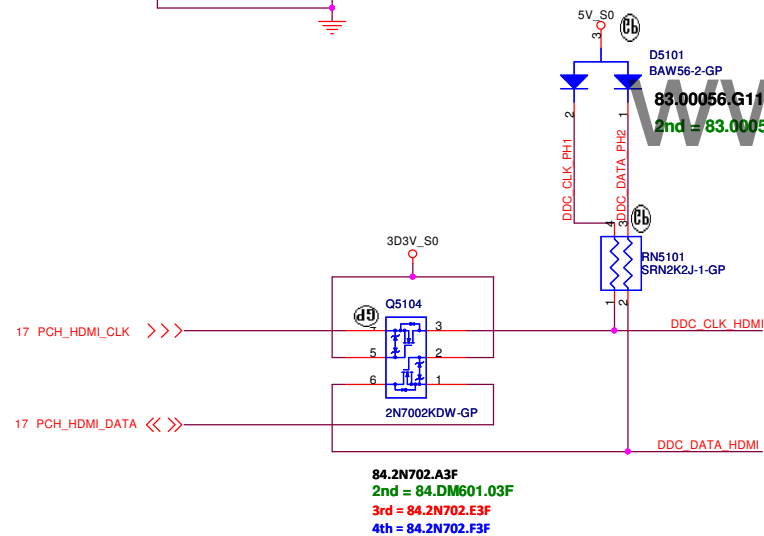
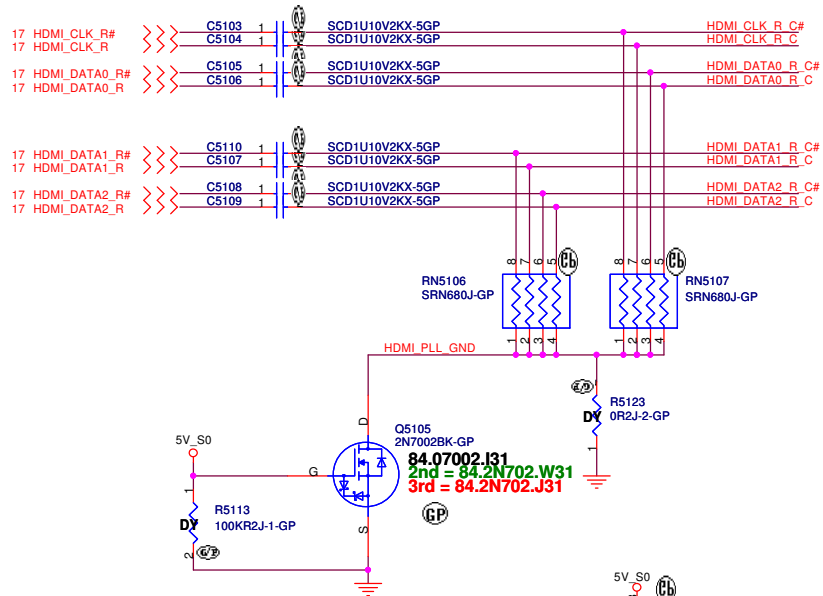
Date: Wednesday, September 05, 2012

Rev
A00

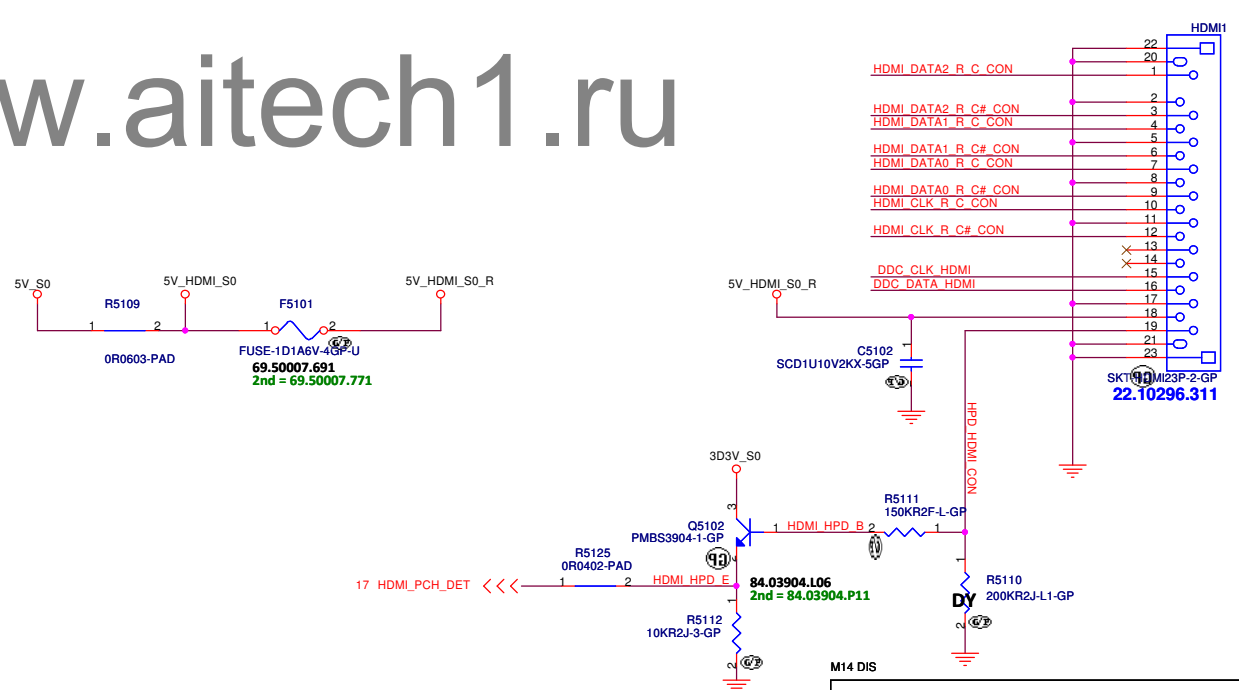
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SSID = VIDEO

HDMI Level Shifter



HDMI CONN



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Title

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LVDS Switch

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Title

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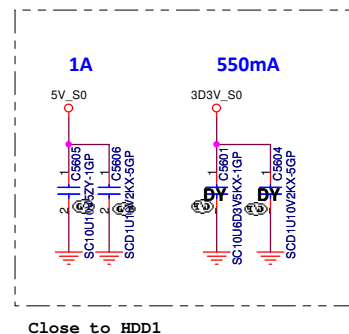
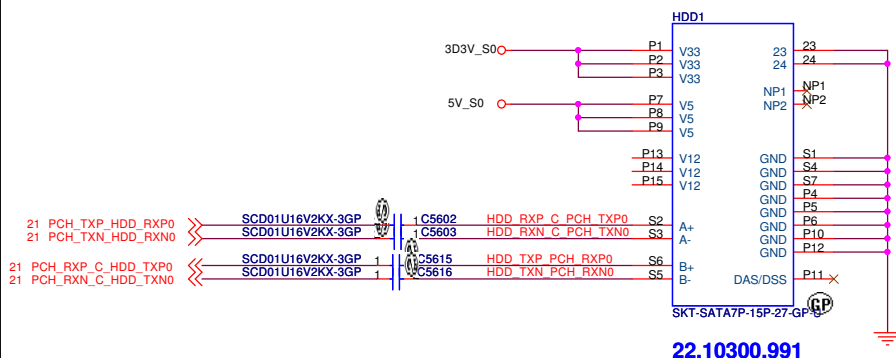
SSID = User.Interface

(Blanking)

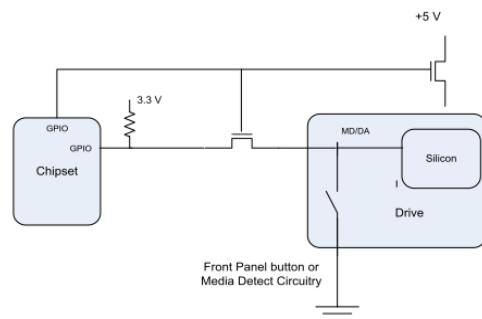
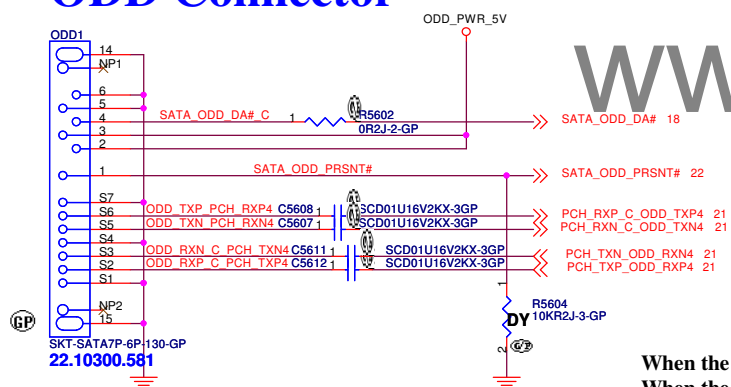
www.aitech1.ru

SSID = SATA

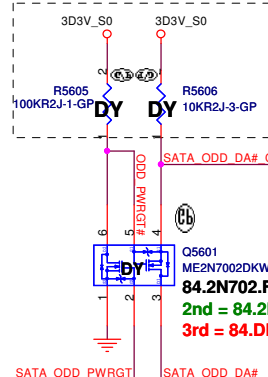
SATA HDD Connector



ODD Connector



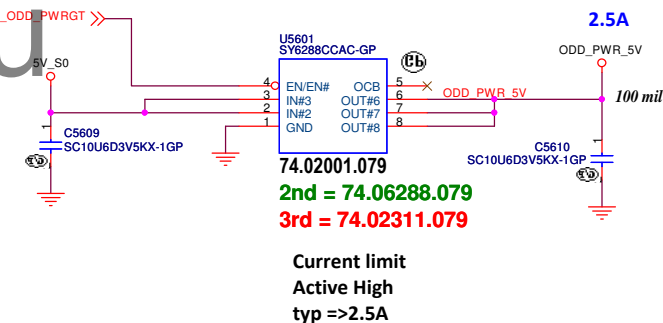
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



A00-0408 Add R5606 to pull high 3.3V_S0
Change pull high to 3.3V_S0

A00-0415 Dummy R5606

SATA Zero Power ODD



Current limit
Active High
typ =>2.5A

M14 DIS

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HDD/ODD		
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SSID = ESATA

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ESATA

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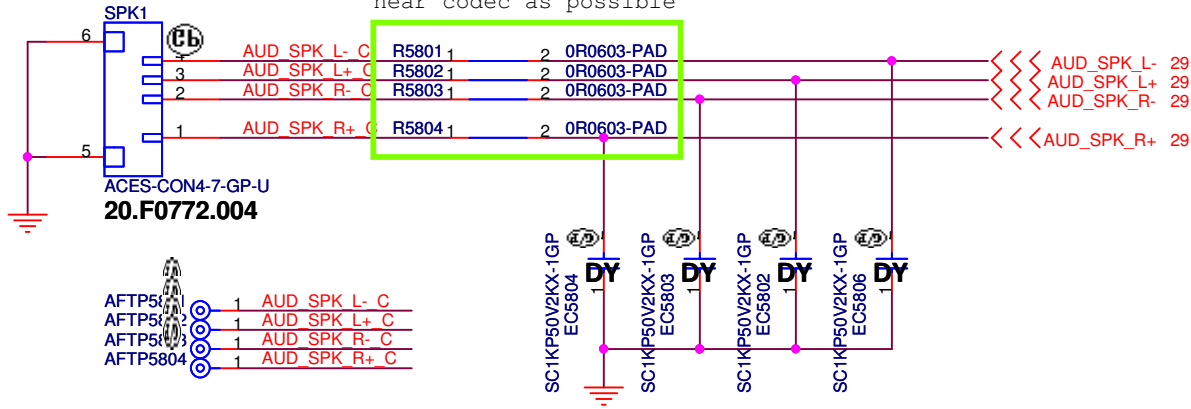
SSID = AUDIO

Speaker

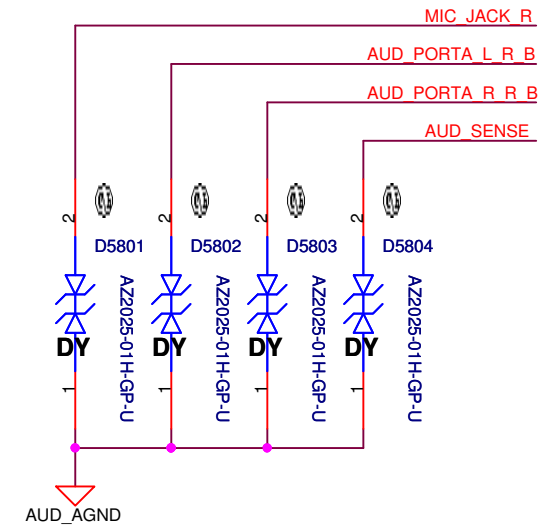
Layout Note:

trace width=30mil

R5801~R5804 and EC5804~EC5806
near codec as possible

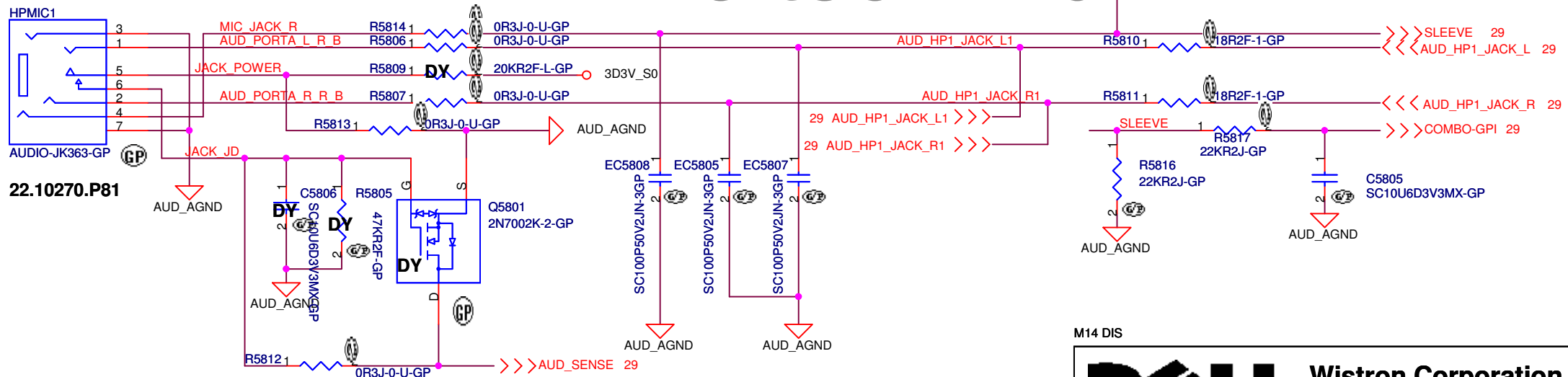


X01 0605



Combo Jack

change to 22.10270.P81, but symble not change



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Speaker/HPMIC CONN

Size
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Document Number

OAK14 Chief River DIS

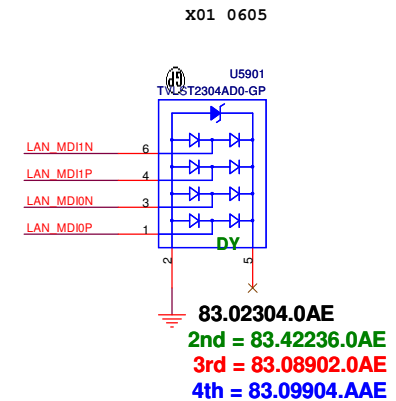
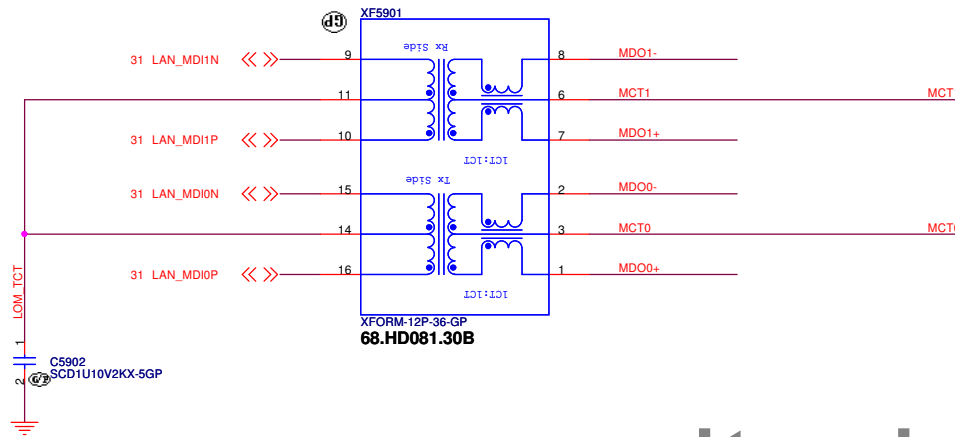
Rev
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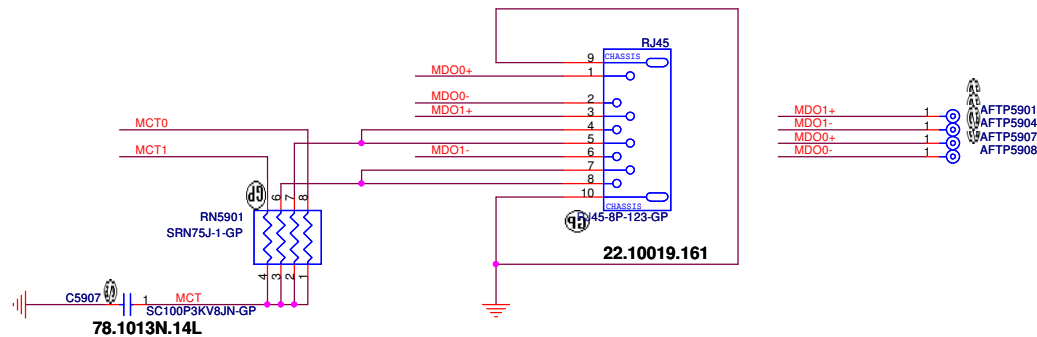
SSID = LOM

LAN TransFormer



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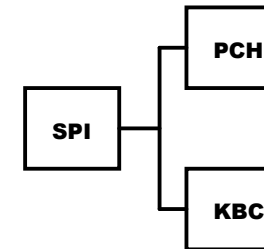
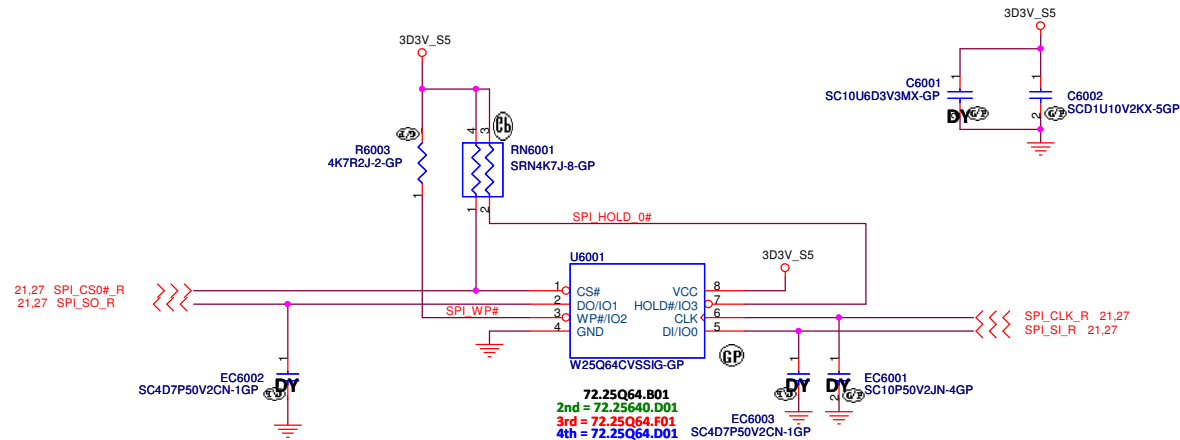
RJ45



<Core Design>

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

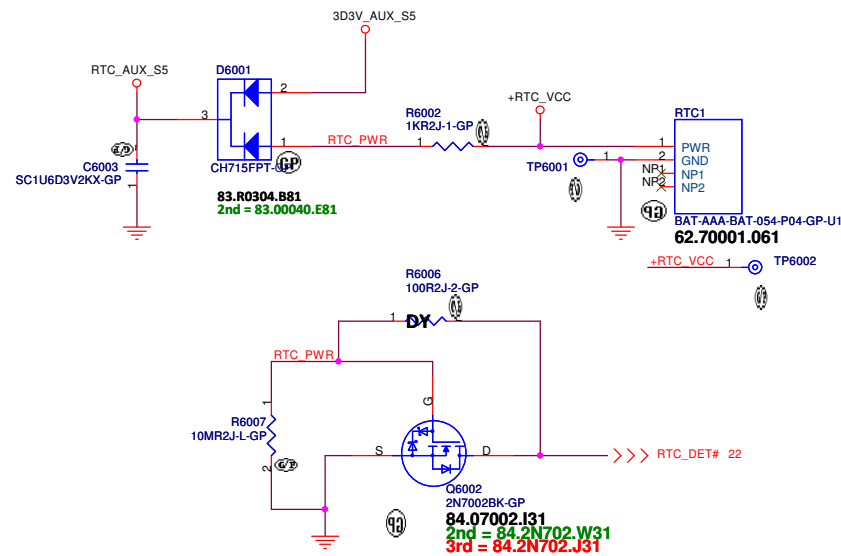


Layout Note:

KBC----10"----PCH
KBC----1.5"~6.5"----SPI
PCH----0.5"~6.5"----SPI

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SSID = RBATT



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Title	Author	Year	Journal	Volume	Page
...

Flash/RTCSize
A3

Document Number

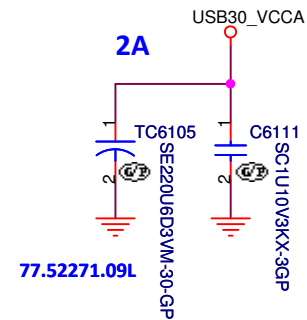
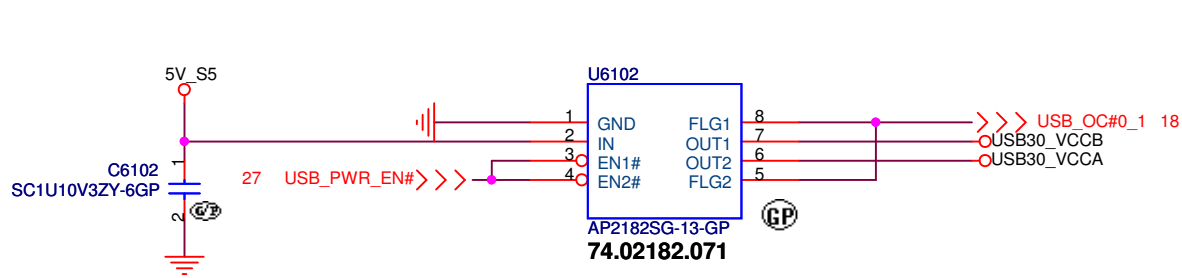
OAK14 Chief River DIS

Rev
400

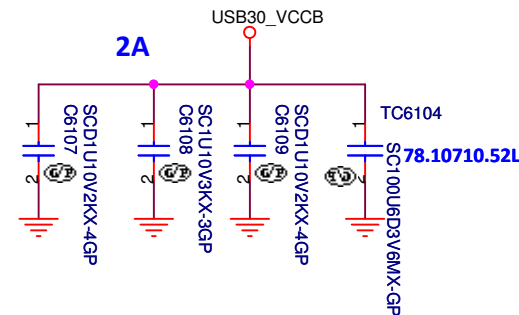
Date: Wednesday, September 05, 2012

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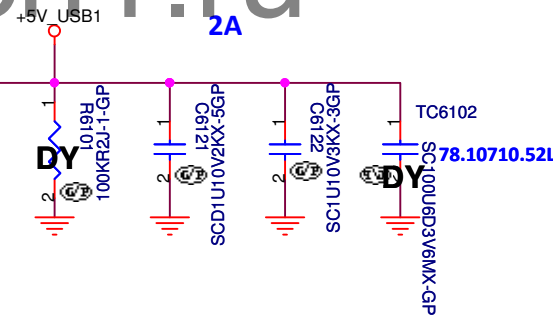
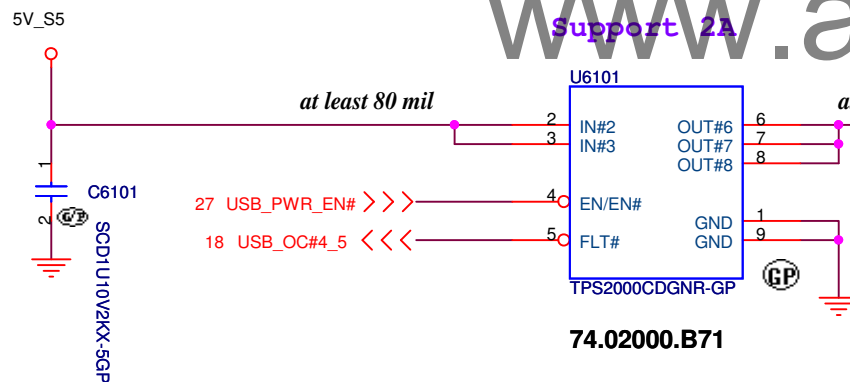
USB3.0 Port1



USB3.0 Port2

Right USB Power x1

Support 2A

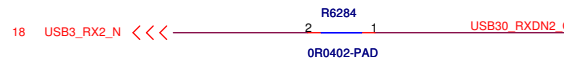
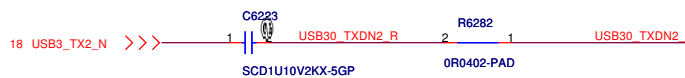
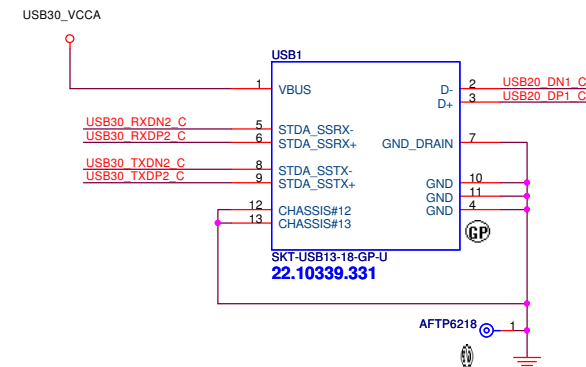
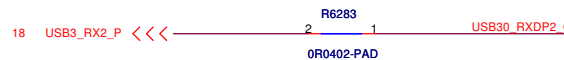
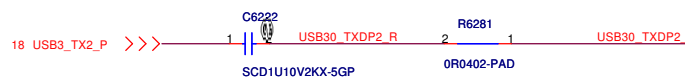
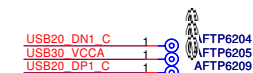
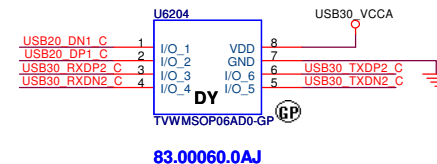
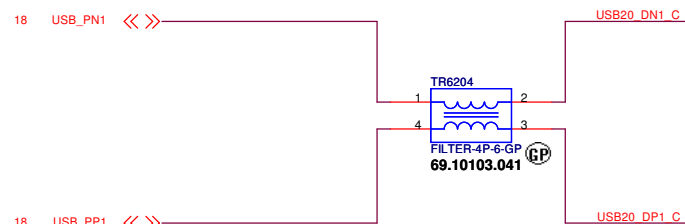


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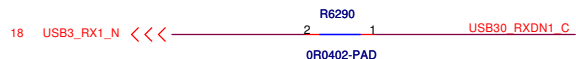
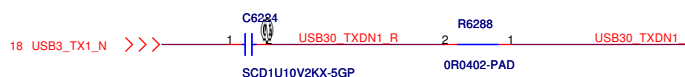
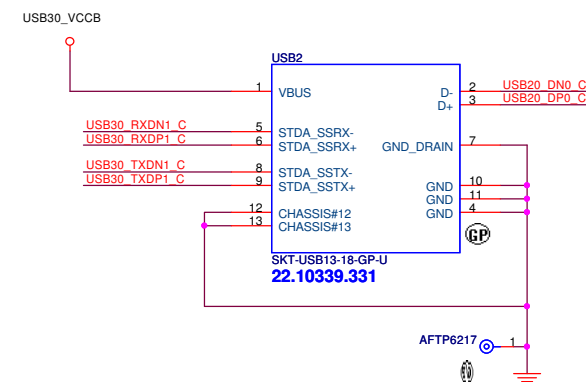
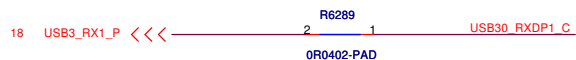
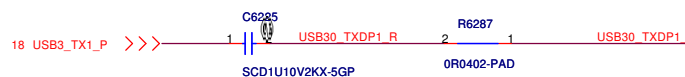
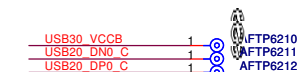
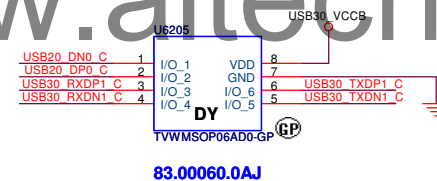
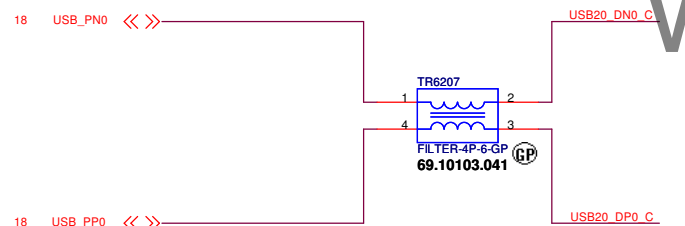
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title USB Power SW	
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SSID = USB

USB3.0 Port1



USB3.0 Port2



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Title

USB 3.0

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SSID = USB

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USB3.0 PORT

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Title

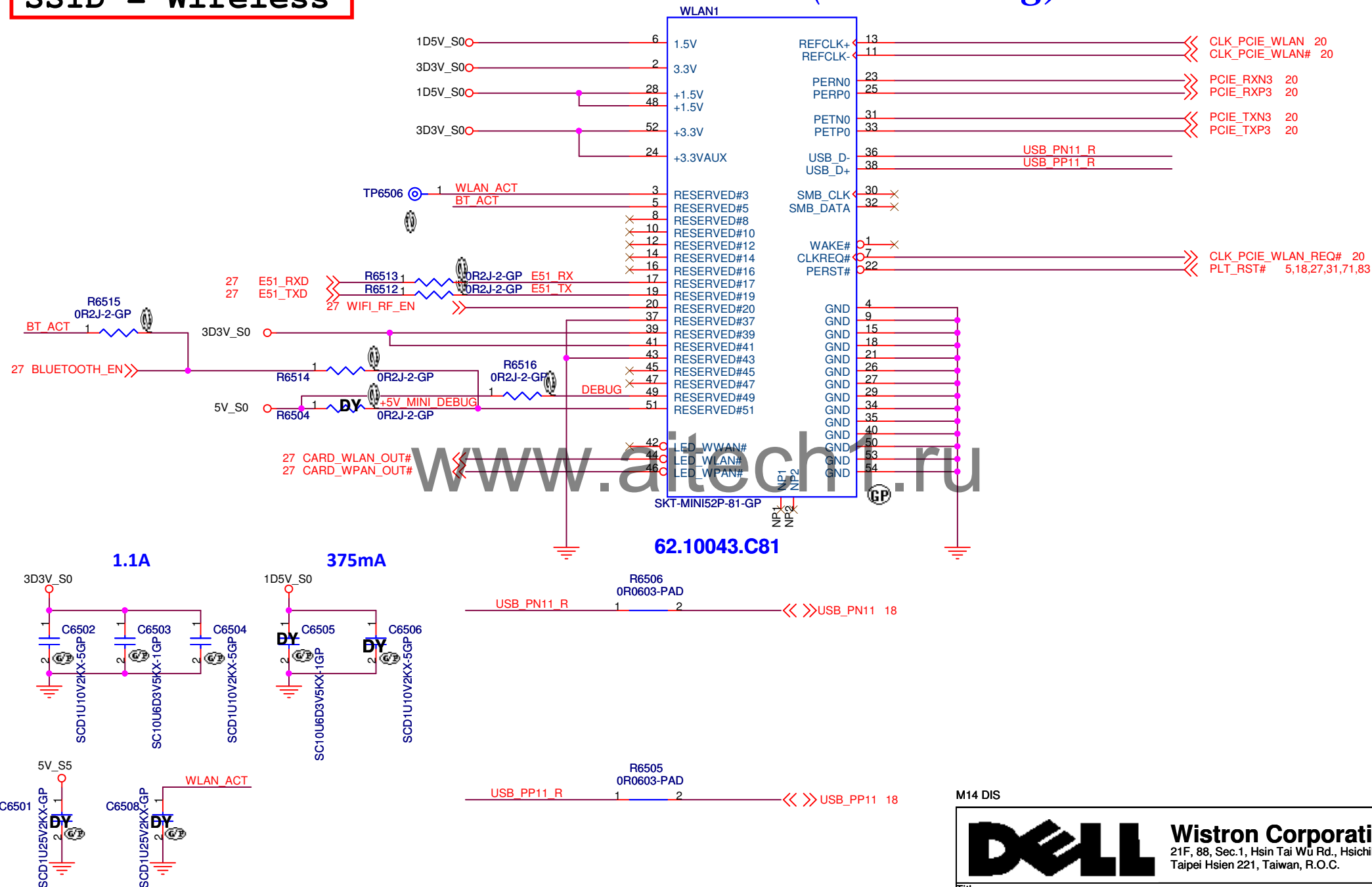
RESERVED

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SSID = Wireless

Mini Card Connector(802.11a/b/g)



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MINICARD(WLAN)/ITP CONN

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Title

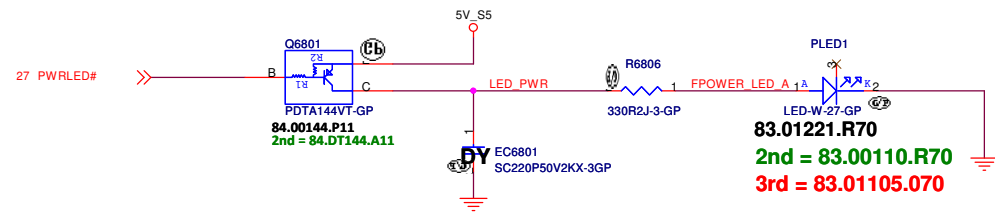
Reserved

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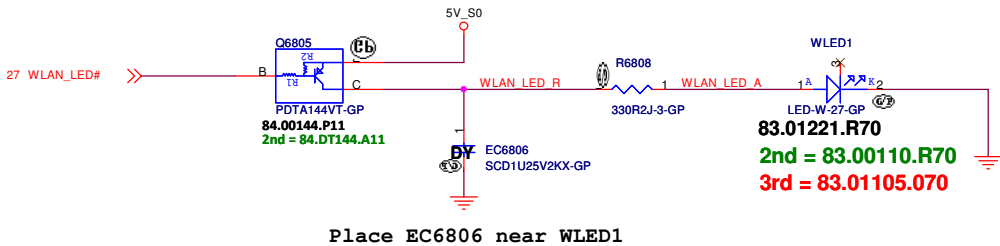
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SSID = User.Interface

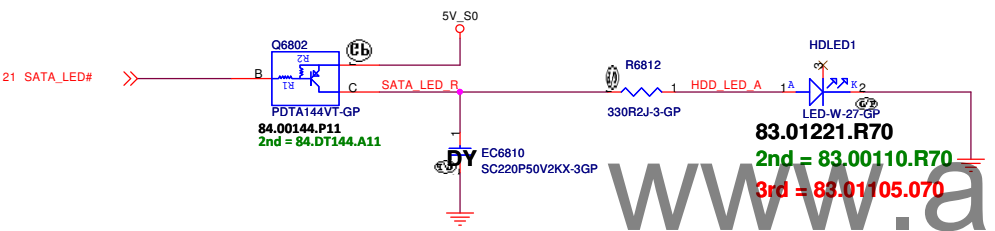
FRONT POWER LED
Low actived from KBC GPIO



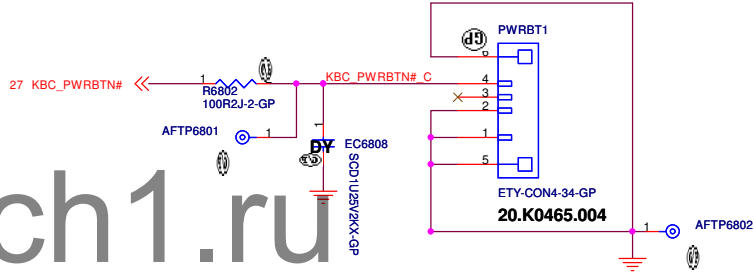
Wireless LED
Low actived from KBC GPIO



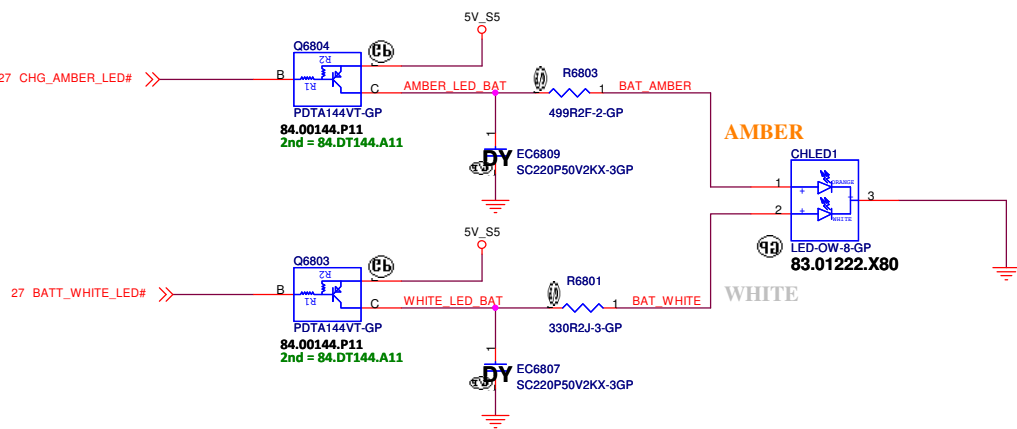
SATA HDD LED(White)
Low actived from PCH GPIO



Power button



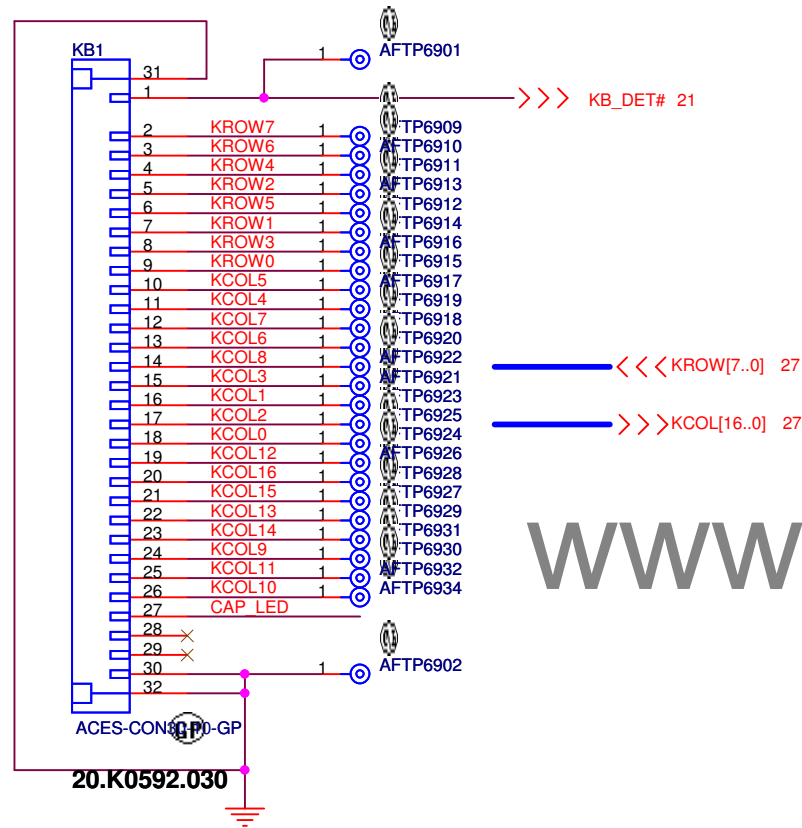
Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

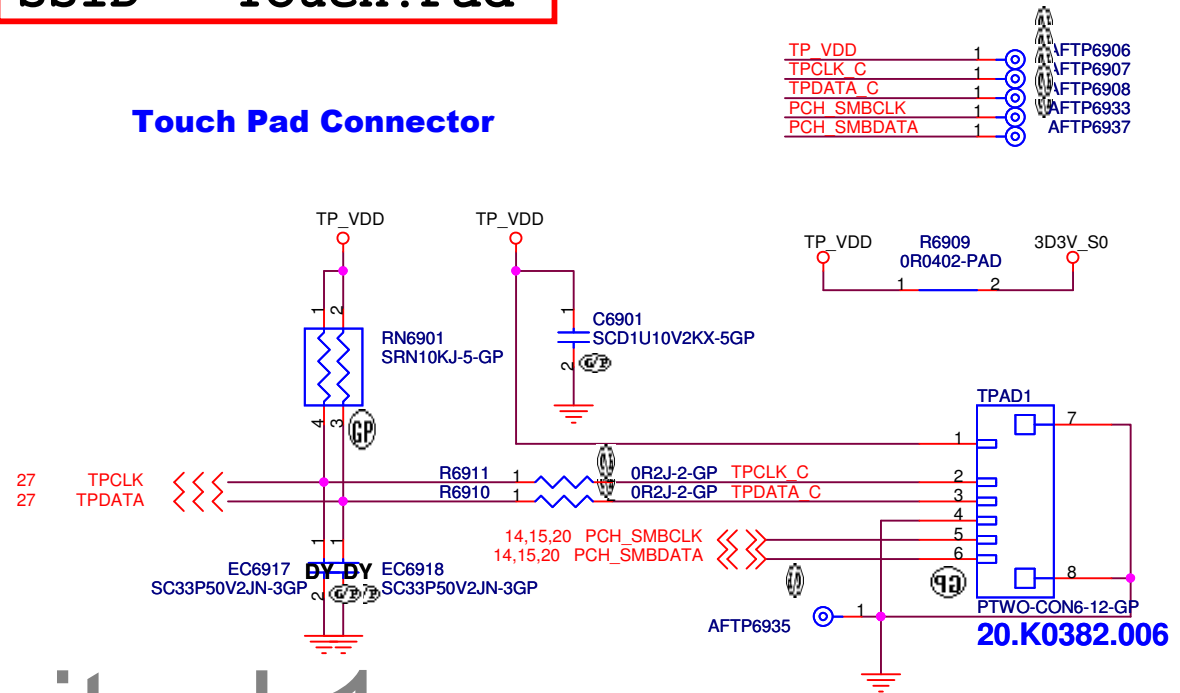
SSID = KBC

Internal Keyboard Connector



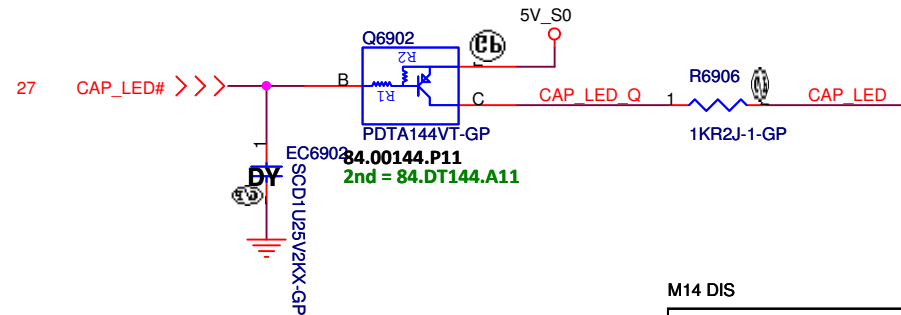
SSID = Touch.Pad

Touch Pad Connector



CAP LED Control

LOW acted from KBC GPIO



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Title

Key Board/Touch Pad

Size

Document Number

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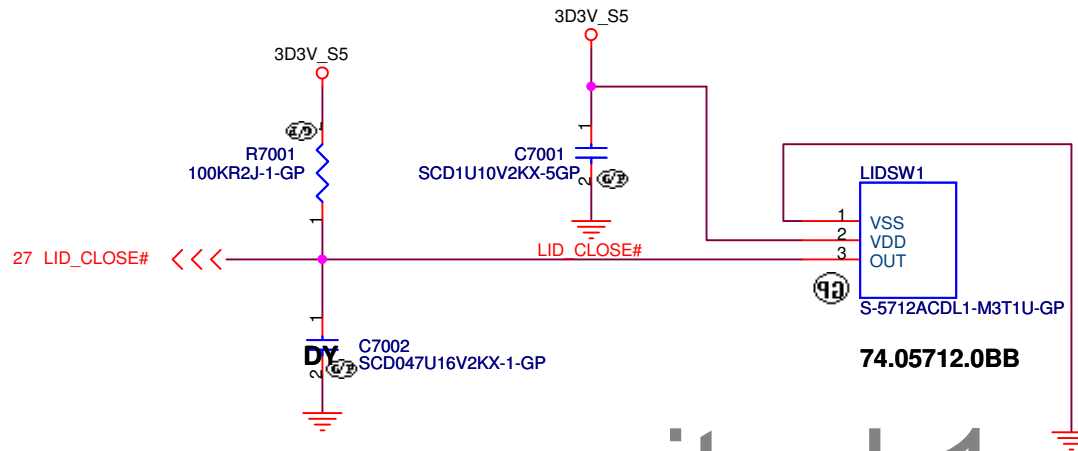
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SSID = User.Interface



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Title

Hall Sensor

Size
A4

Document Number

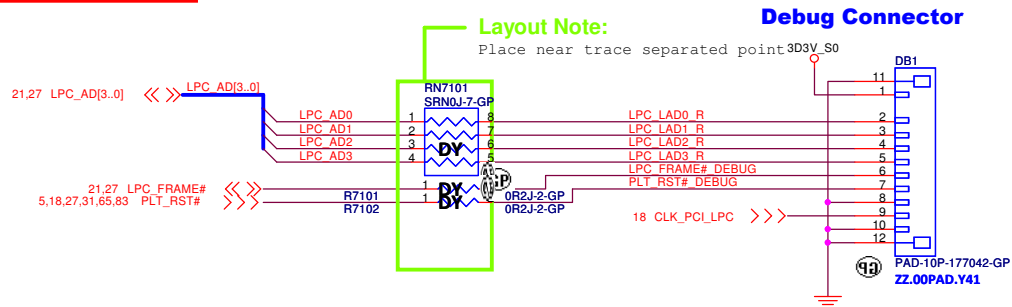
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SSID = DEBUG PORT



SSID = CPU

CPU XDP




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Title			
Dubug connector			
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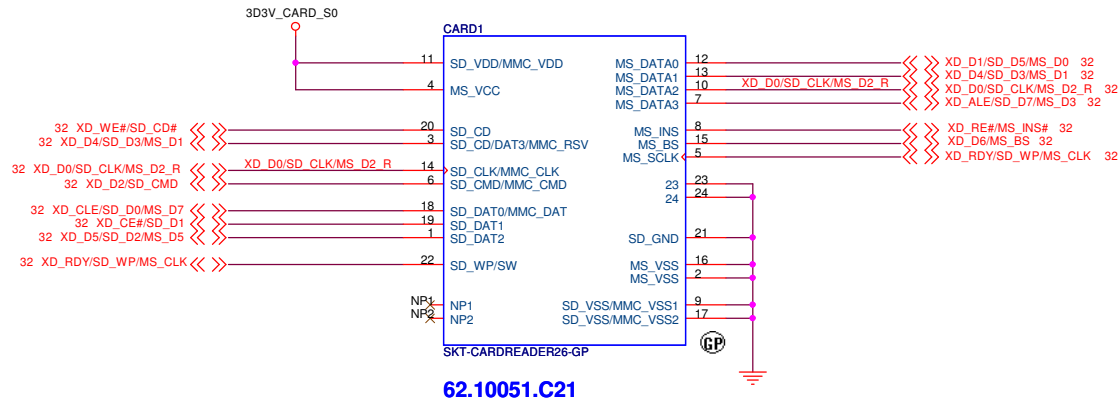
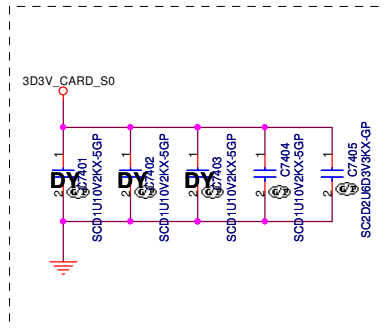
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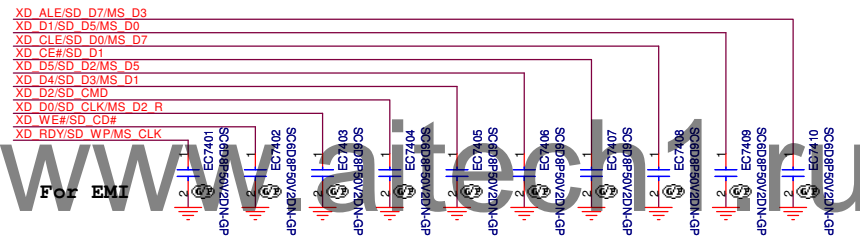
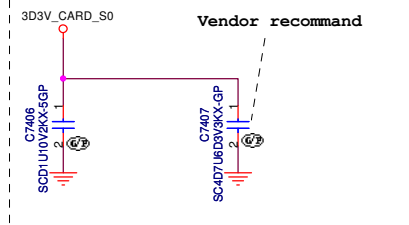
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SSID = SDIO



Close to Socket



M14 DIS

[illegible]

SD/XD/MS/MMC Card CONN

Size

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Title			
Express Card			
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Title

Free Fall Sensor

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Title

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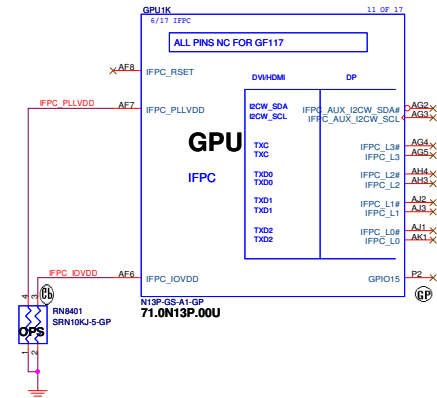
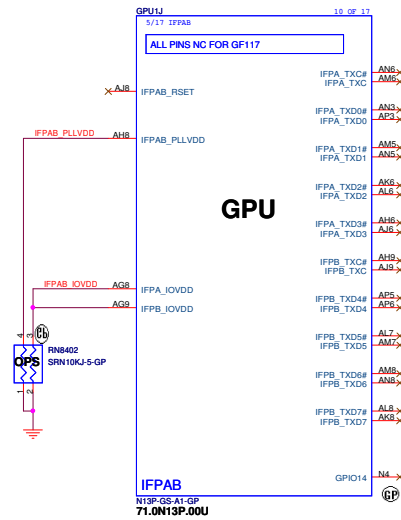
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SSID = User.Interface

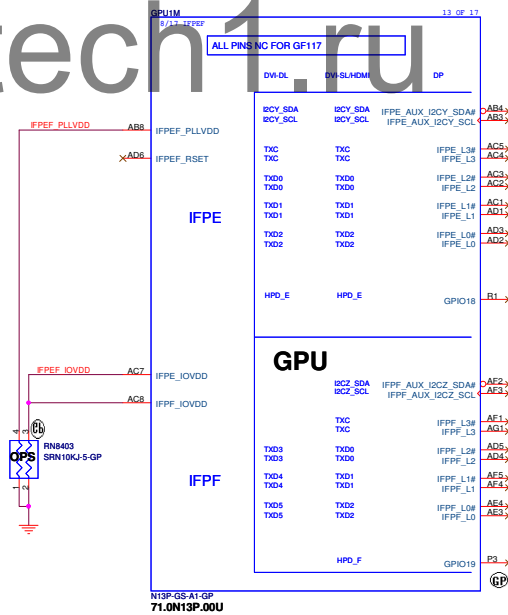
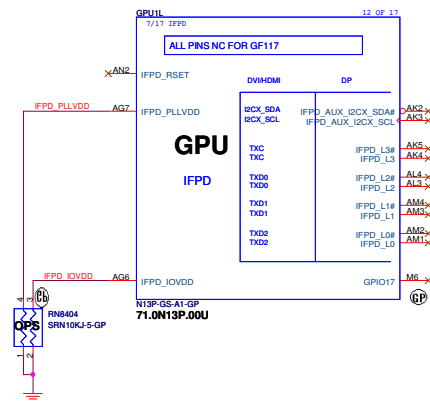


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LVDS Interface

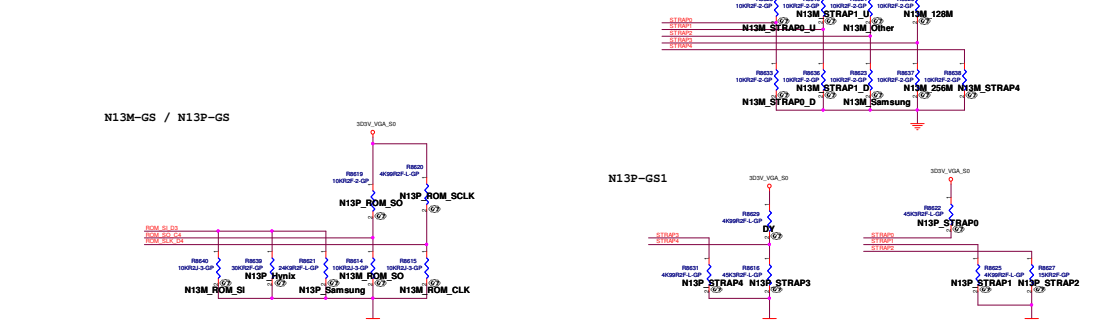
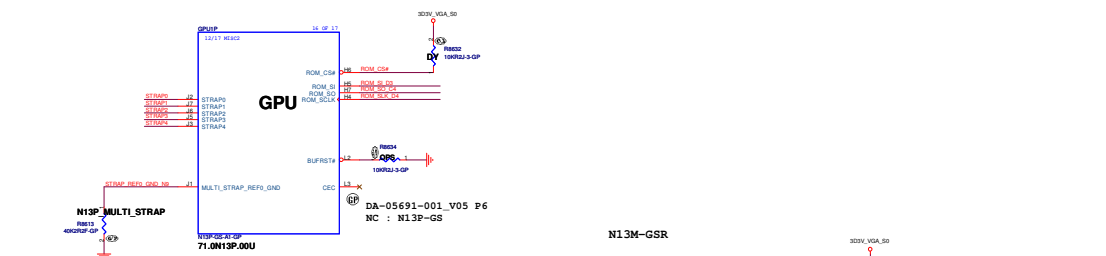
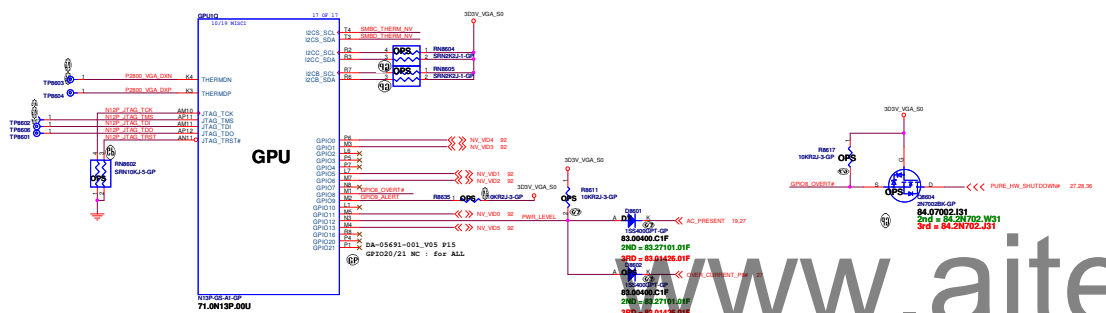
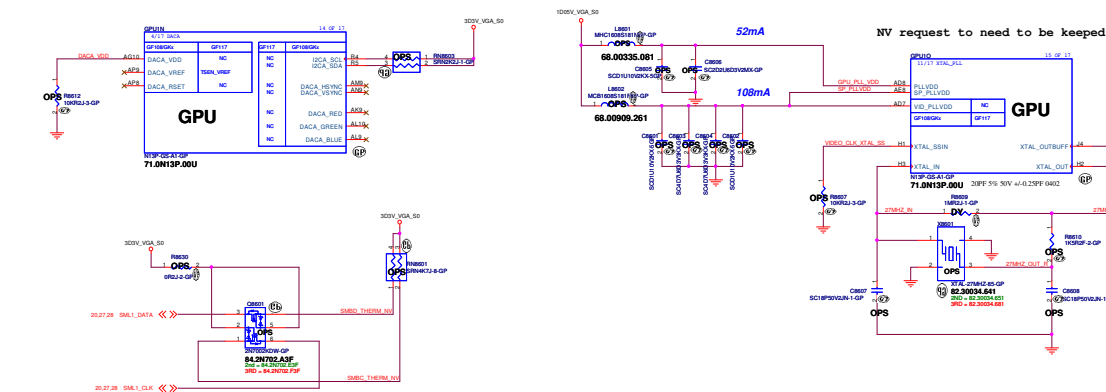


HDMI Interface



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M14 DIS



N13P-GS1

Strap Pin Name	Logical strapping name bit#1	Logical strapping name bit#2	Logical strapping name bit#3	Logical strapping name bit#4
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_M
ROM_SI	RAM_CFG[2]	RAM_CFG[2]	RAM_CFG[2]	RAM_CFG[2]
ROM_SO	FB[1]	FB[1]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	SGIO_PADCFG[3]	SGIO_PADCFG[2]	SGIO_PADCFG[1]	SGIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SORR_EXPOSED	SORR2_EXPOSED	SORR1_EXPOSED	SORR_EXPOSED
STRAP4	RESERVED	PCISPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

GPU	N13P-GS
STRAP 0	PULL UP 45.3K
STRAP 1	PULL DOWN 4.99K
STRAP 2	PULL DOWN 15K
STRAP 3	PULL DOWN 4.99K
STRAP 4	PULL DOWN 45.3K
ROM_SO	PULL UP 10K
ROM_SCLK	PULL UP 4.99K
VRAM	ROM_SI pin
128M*16 DDR3 Samsung K4W2G1646E-BC11	Pull down 24.9K ohm
128M*16 DDR3 Hynix H5TQ2G63DFR-11C	Pull down 30K ohm

Part Reference	Part Number	Value	PCB Footprint
R8621 (DIS_ROM SI)	64.20025.6DL 20K R2F-L-GP	R402H16	
R8621	64.15025.6DL 15K R2F-L-GP	R402H16	
R8621	64.34825.6DL 34.8K R2F-L-GP	R402H16	
R8621	64.45325.6DL 45.3K R2F-L-GP	R402H16	
R8621	64.30125.6DL 30K R2F-L-GP	R402H16	
R8621	64.24925.6DL 24.9K R2F-L-GP	R402H16	

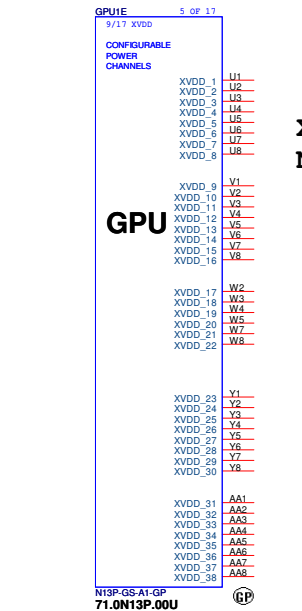
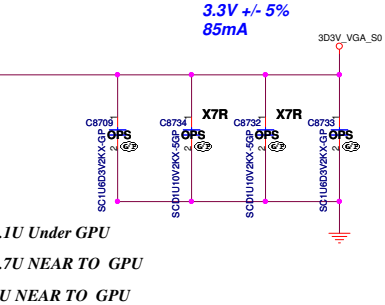
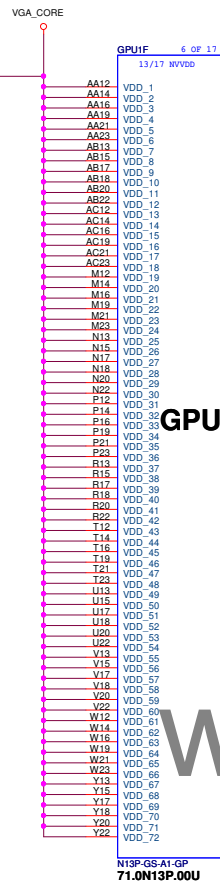
Table 4. Binary Strap Mode Mapping

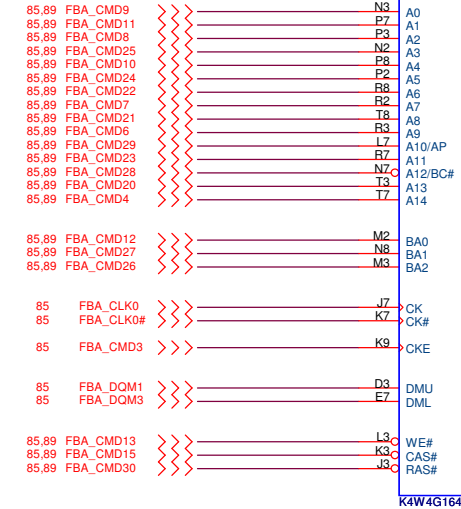
Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

GPU	N13M-GS			
STRAP 4	PULL DOWN 10K			
ROM_SCLK	PULL DOWN 10K			
ROM_SO	PULL DOWN 10K			
ROM_SI	PULL DOWN 10K			
VRAM	STRAP 0	STRAP 1	STRAP 2	STRAP 3
128M*16 DDR3 Samsung	PULL UP 10K	PULL UP 10K	PULL DOWN 10K	PULL UP 10K
128M*16 DDR3 Hynix	PULL DOWN 10K	PULL DOWN 10K	PULL UP 10K	PULL UP 10K
256M*16 DDR3 Samsung	PULL UP 10K	PULL DOWN 10K	PULL DOWN 10K	PULL DOWN 10K
256M*16 DDR3 Micron	PULL UP 10K	PULL DOWN 10K	PULL UP 10K	PULL DOWN 10K

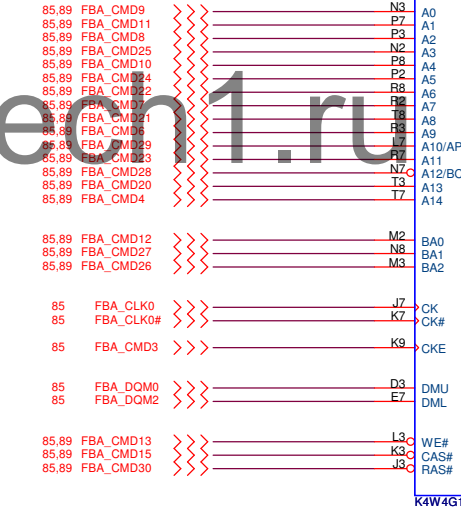
4/9 update GPU strapping

VGA_CORE

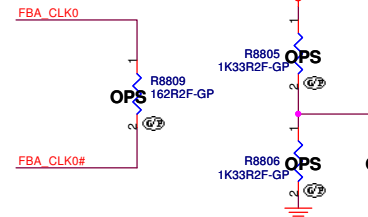


[illegible]

72.4164



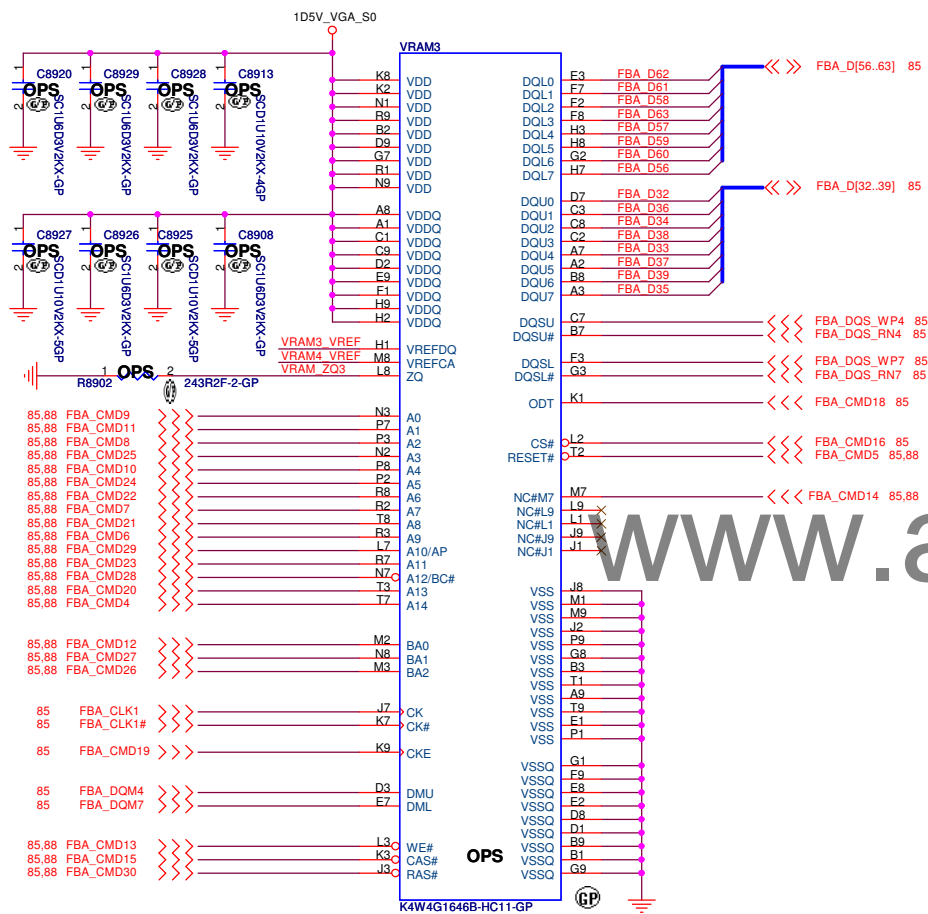
72.410



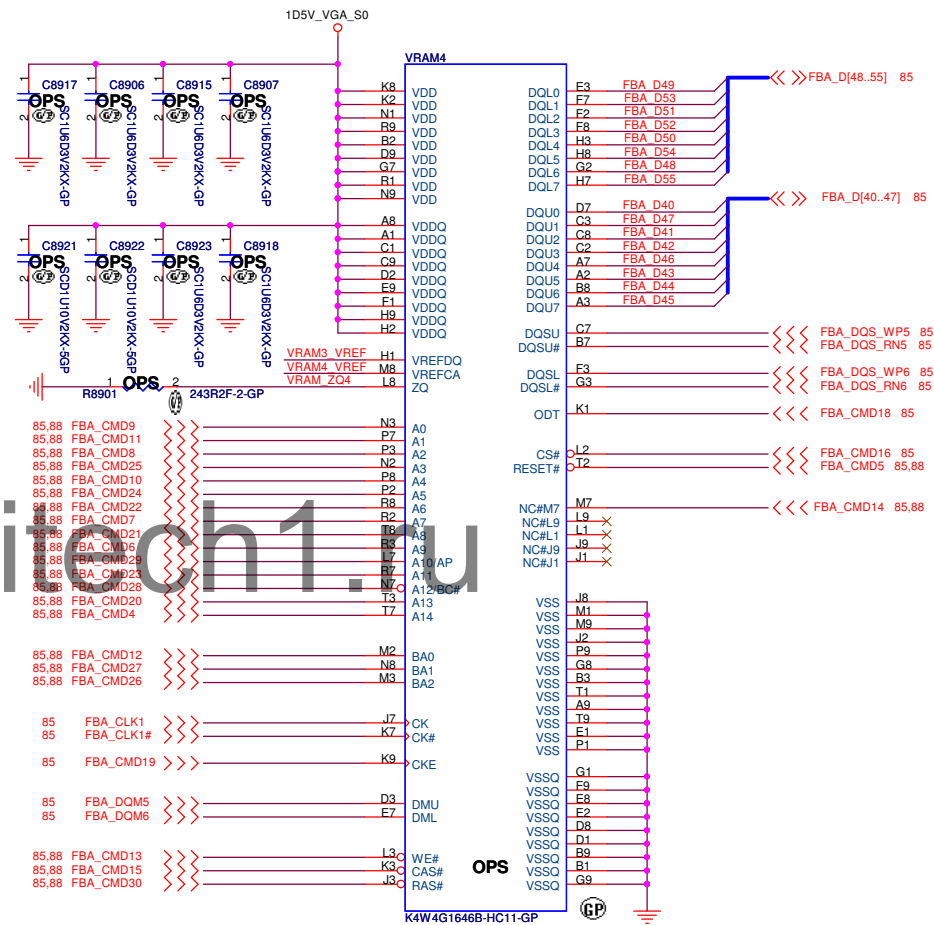
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM1,2 (1/4)			
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Title			
GPU-VRAM1,2 (1/4)			
Size A3	Document Number	Rev	
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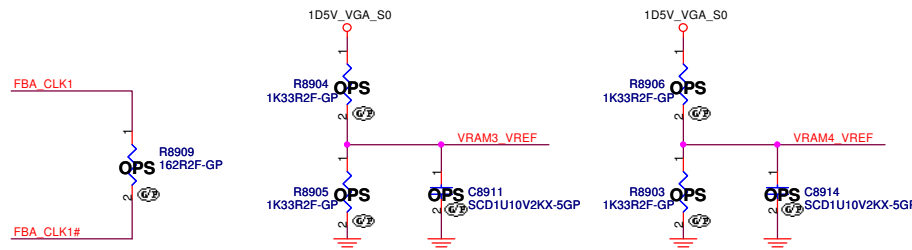
Frame Buffer Patition A-Upper Half



72.41646.00U



72.41646.00U



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Title **GPU-VRAM3,4 (2/4)**
Size A3 Document Number **OAK14 Chief River DIS** Rev **A00**
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Frame Buffer Partition B-Upper Half

The diagram illustrates the Frame Buffer Partition B-Upper Half, featuring two 8VRAM chips (VRAM7 and VRAM8) connected to a K4W4G1646B-HC11-GP. The schematic shows detailed pin connections for data, address, and control signals, as well as power and ground connections. A large watermark "www.aih1.com" is overlaid on the center.

VRAM7 Pin Connections:

- Data Bus:** DQ0-DQ7, DQS#, DQSL#, ODT, CS#, RESET#
- Address Bus:** A0-A14
- Control Signals:** WE#, CAS#, RAS#, DMU, DML
- Power/Ground:** VDD, VDDQ, VSS, VSSQ
- Other:** VRAM7 VREF, VRAM8 VREF, VRAM_ZQ7

VRAM8 Pin Connections:

- Data Bus:** DQ0-DQ7, DQS#, DQSL#, ODT, CS#, RESET#
- Address Bus:** A0-A14
- Control Signals:** WE#, CAS#, RAS#, DMU, DML
- Power/Ground:** VDD, VDDQ, VSS, VSSQ
- Other:** VRAM7 VREF, VRAM8 VREF, VRAM_ZQ8

Power and Ground Connections:

- 1D5V_VGA_S0:** Connected to VDD and VDDQ of both VRAM chips.
- VRAM7 VREF:** Connected to VREFDQ and VREFCA of VRAM7.
- VRAM8 VREF:** Connected to VREFDQ and VREFCA of VRAM8.
- VRAM_ZQ7/ZQ8:** Connected to ZQ pins of VRAM7 and VRAM8.

Component Values:

- VRAM7:** 8VRAM, 243R2F-2-GP
- VRAM8:** 8VRAM, 243R2F-2-GP
- VRAM7 VREF:** 1U10V2KX-5GP
- VRAM8 VREF:** 1U10V2KX-5GP

Part Numbers:

- VRAM7:** 72.41646.00U
- VRAM8:** 72.41646.00U

Additional Components:

- R9103, R9105, R9106, R9107:** 1K33R2F-GP
- R9109, R9110, R9111, R9112:** 1U10V2KX-5GP

Legend:

- VRAM7:** 8VRAM
- VRAM8:** 8VRAM

Notes:

- VRAM7 VREF, VRAM8 VREF, VRAM_ZQ7, VRAM_ZQ8

Footer:

M14 DIS

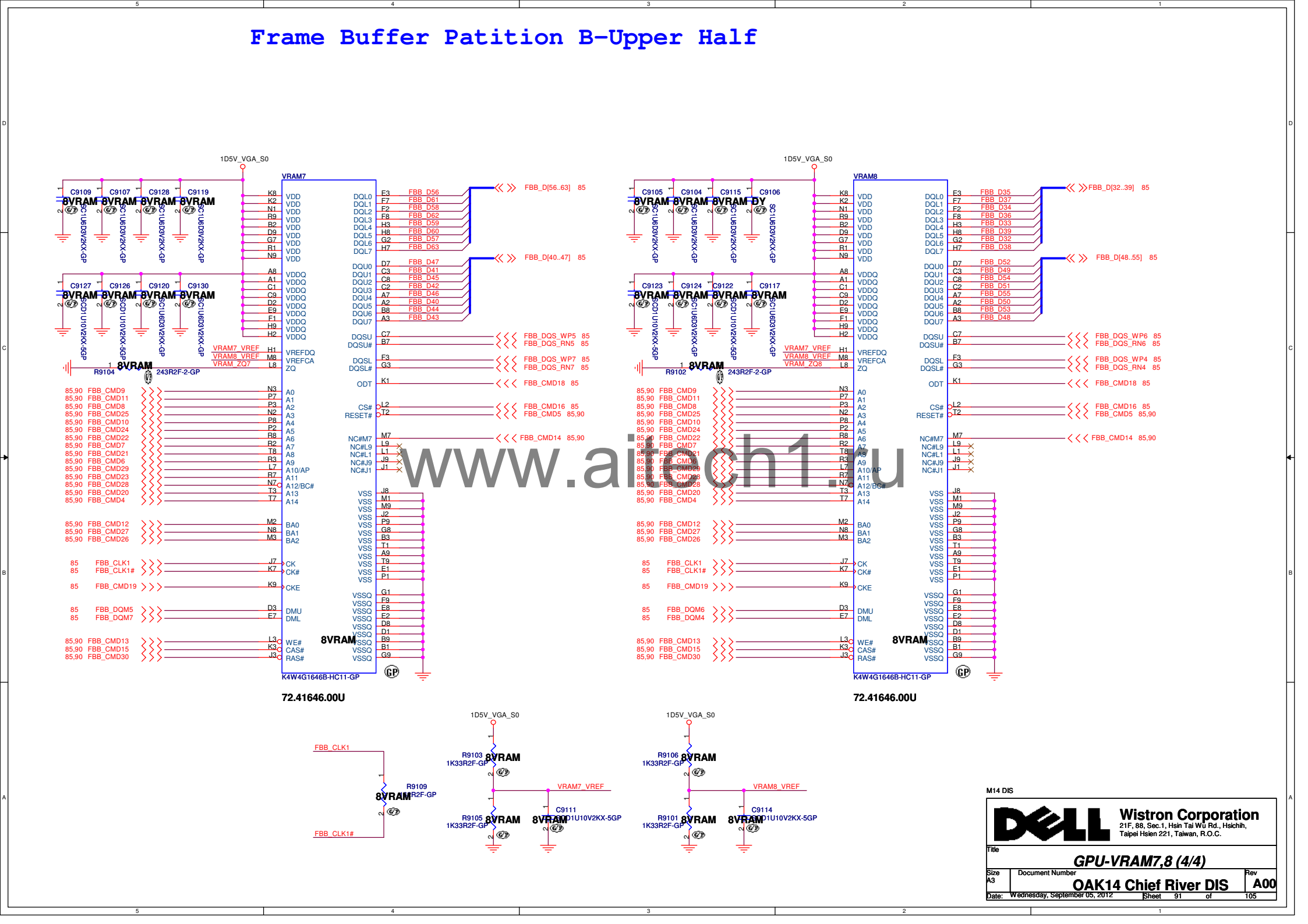
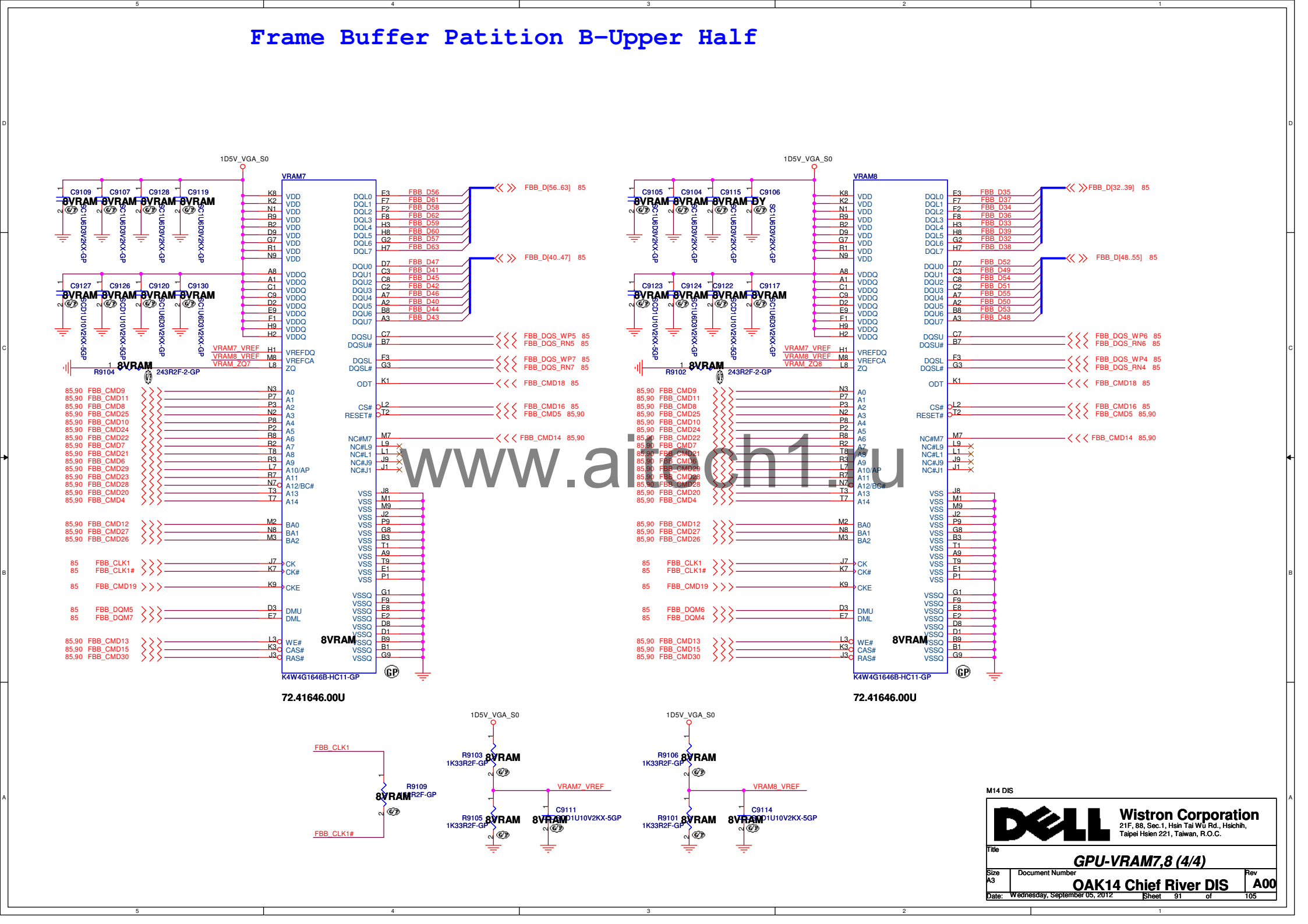
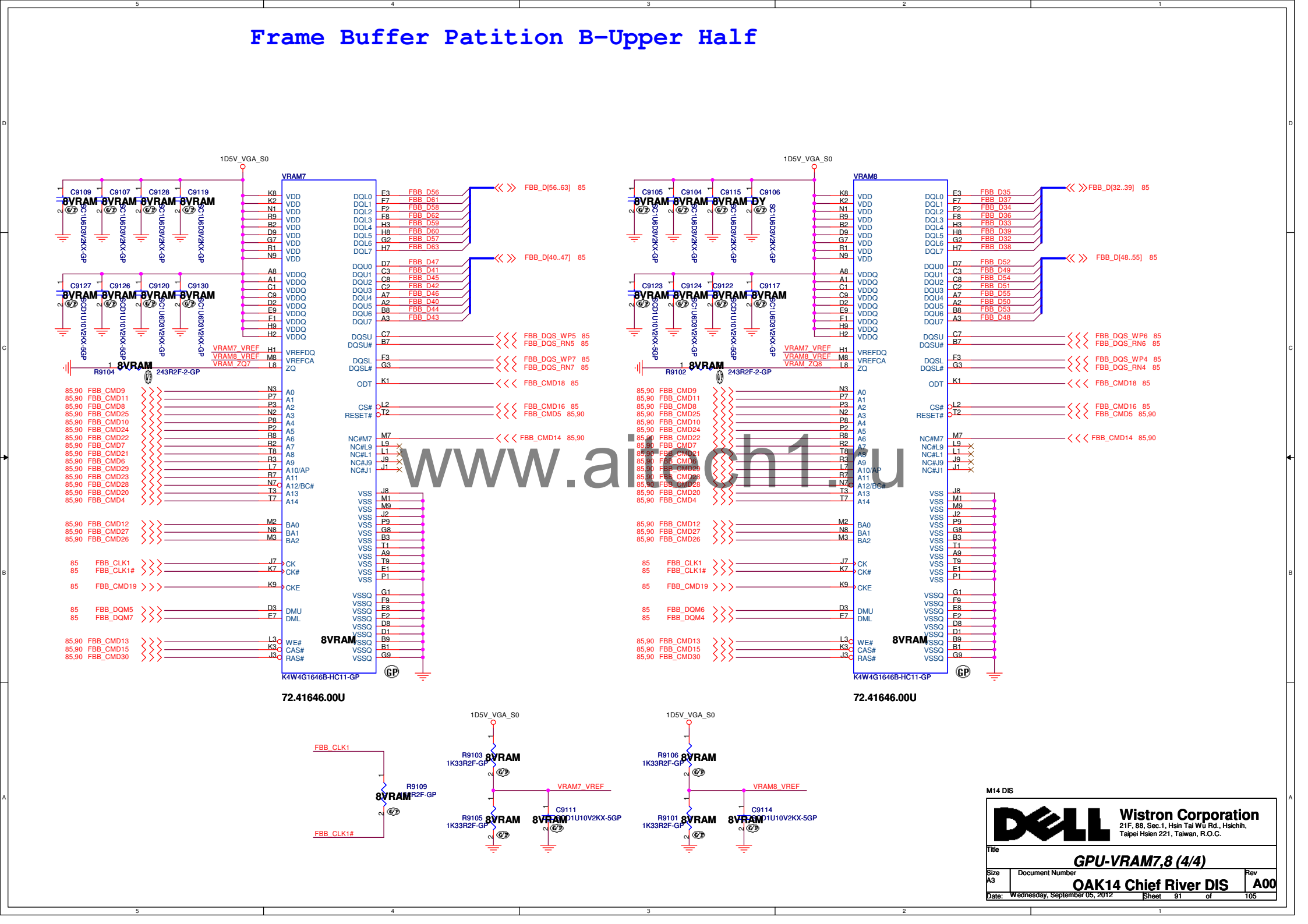
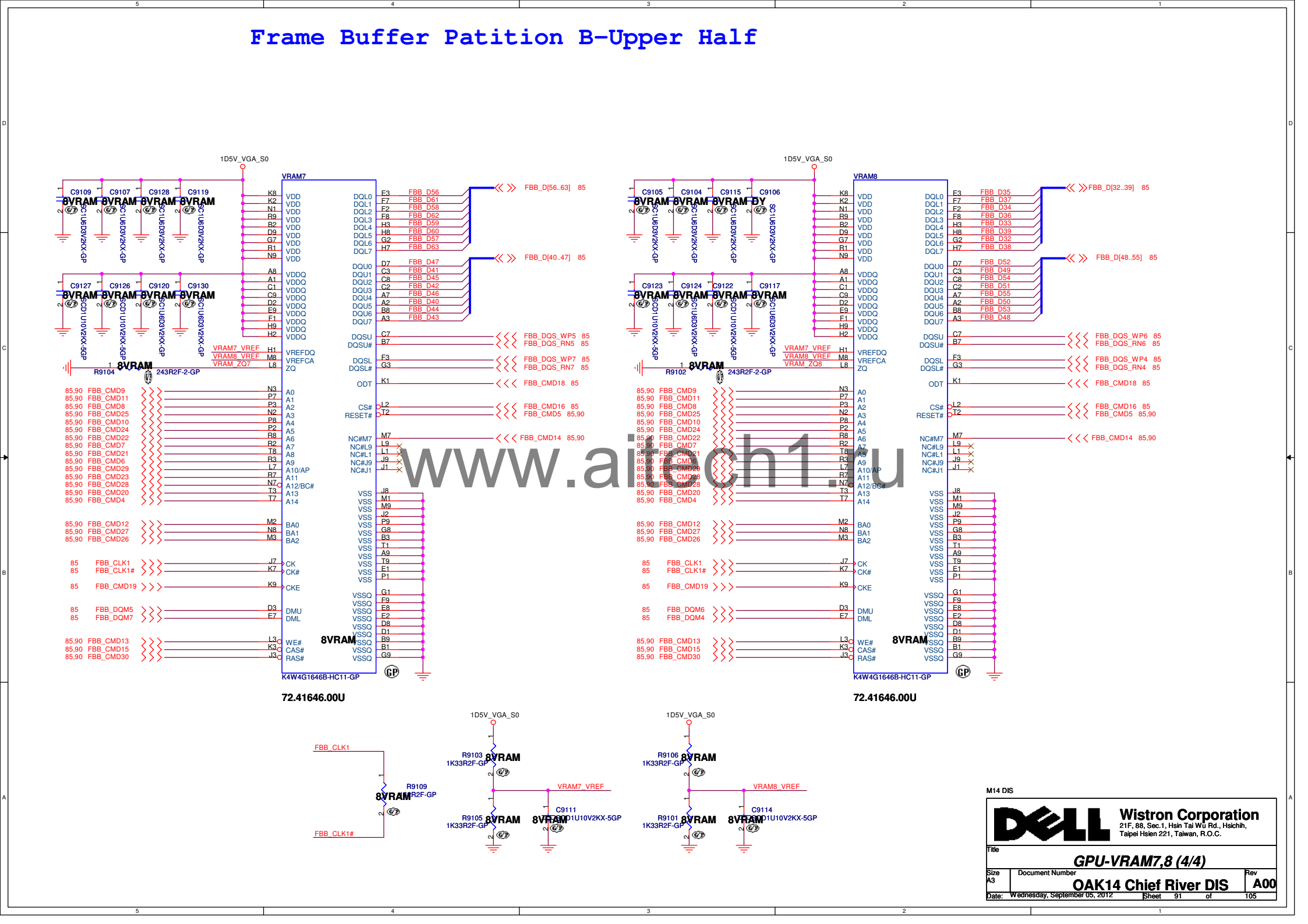
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GPU-VRAM7,8 (4/4)

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Title

LVDS Switch

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Title

CRT Switch

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SSID = SDIO

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Title

TOUCH PANEL

Size
A3

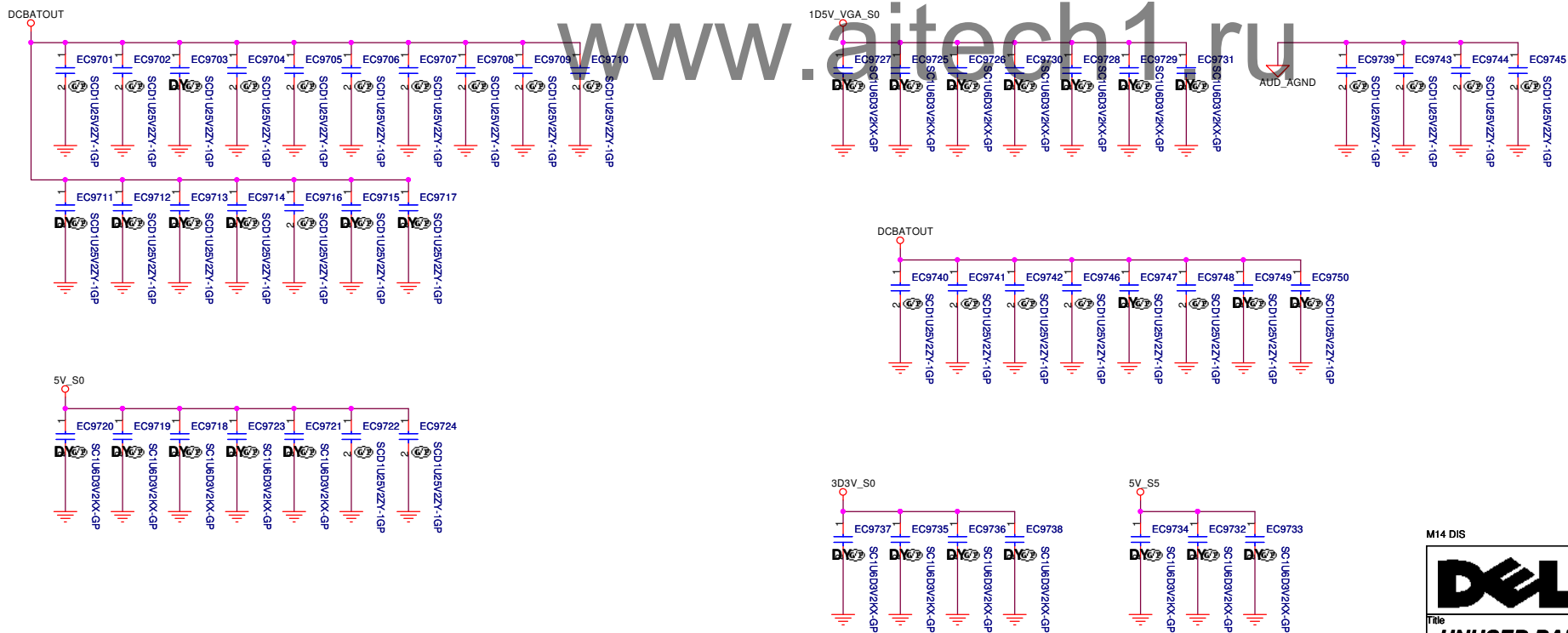
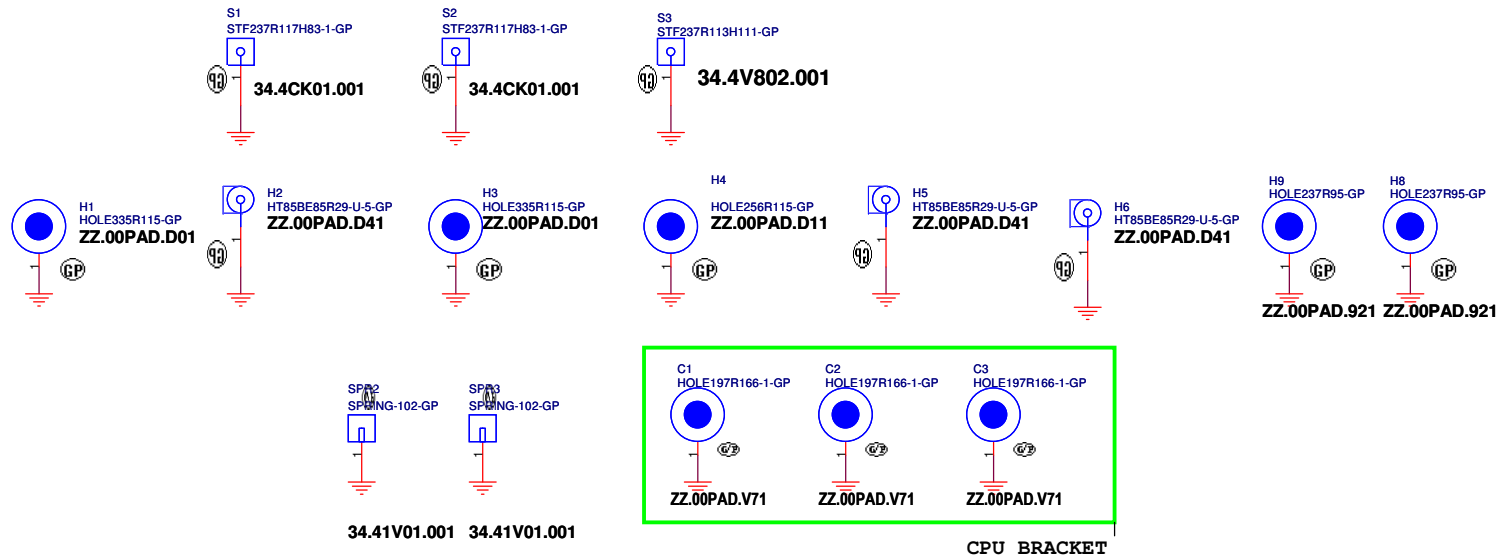
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SSID = EMI



(AC mode)

Within logic high level and disable :
it is less than the logic low level.

Ta

VREF_{bus} must be powered up before Vcore₃, or after Vcore₃ within 0.7 V. Also, VREF_{bus} must power down after Vcore₃, or before Vcore₃ within 0.7 V.

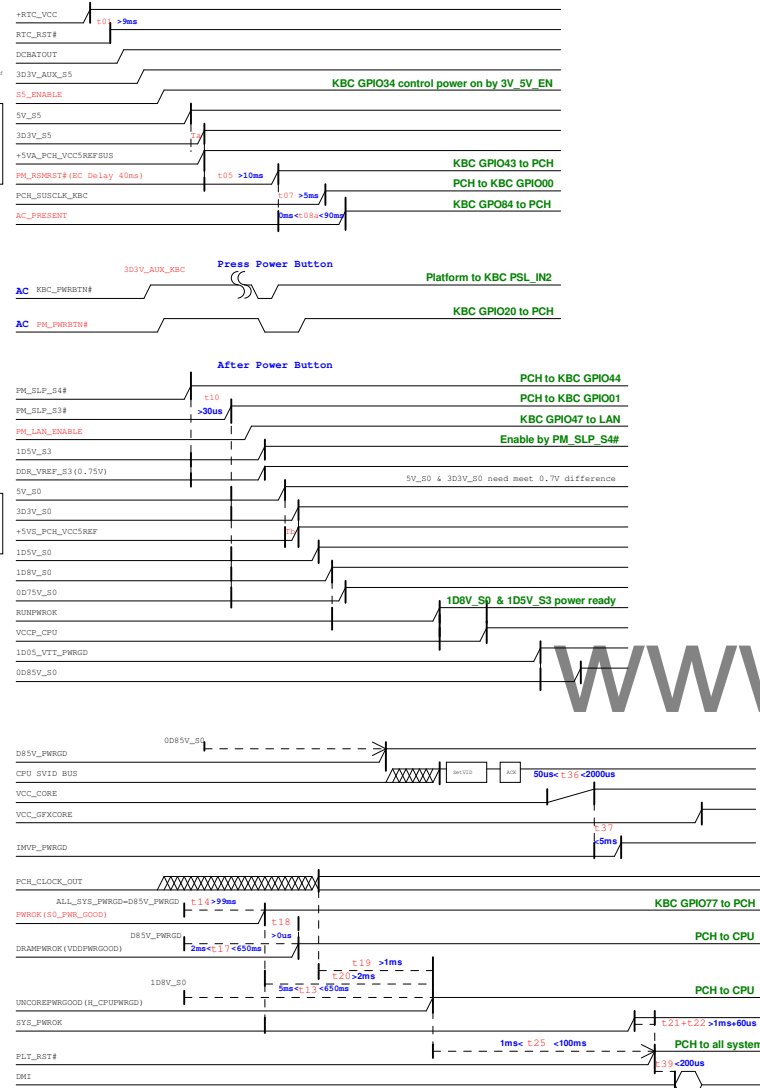
Not floating.

sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

Tb
VIRF must be powered up before Voc1_3, or after Voc1_3 within 0.7 V. Also, VIRF must power down after Voc1_3, or before Voc1_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



Timing diagram for PCH GPIO54 output. The diagram shows the sequence of events for power down, including the first rail to power down and the last rail to power down, with specific timing constraints like $<10ms$ and $>0ms$.

Signals shown:

- GPIO_PWR_EN# (Discrete only)
- 3D3V_VGA_S0 (VDD33)
- #208A_EN#/DIM_VGA (Discrete only)
- VGA_CORE (FVVDQ)
- GPIO_PWBOK (Discrete only)
- 1D5V_VGA_S0 (FVVDQ)
- 1D5V_VGA_S0 (PEX_VD)
- 1D5V_VGA_S0 (PEX_VD)
- V1V-V1VQDQ

Timing constraints:

- $<10VVDQ > 0ms$
- $<10V - FVVDQ > 0ms$
- $<10V - PEX_VD > 0ms$
- $t_{POWER-OFF} < 10ms$

Labels:

- PCH GPIO54 output
- RT8208 PG000
- VGA_CORE, 1D5V_VGA_S0, 3D3V_VGA_S0

(DC mode)

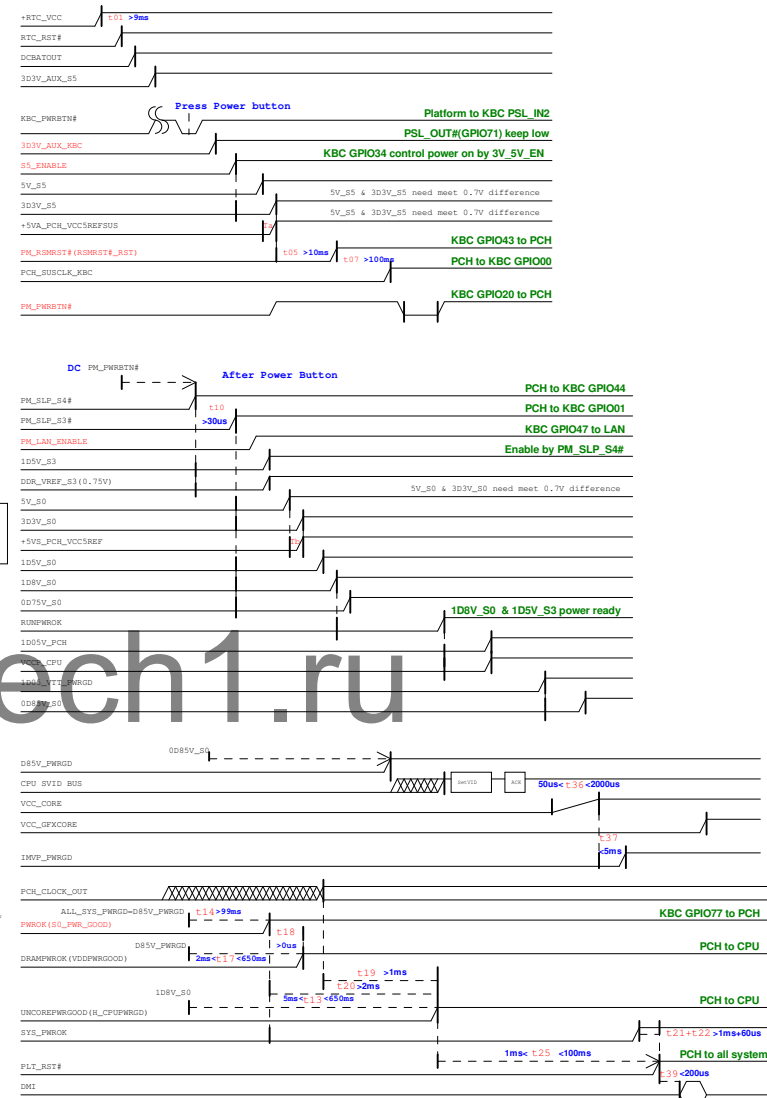
Sense the power button status

VREF_Sus must be powered up before VccSus3_3, or after VccSus3_3 with 0.7 V. Also, VREF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.

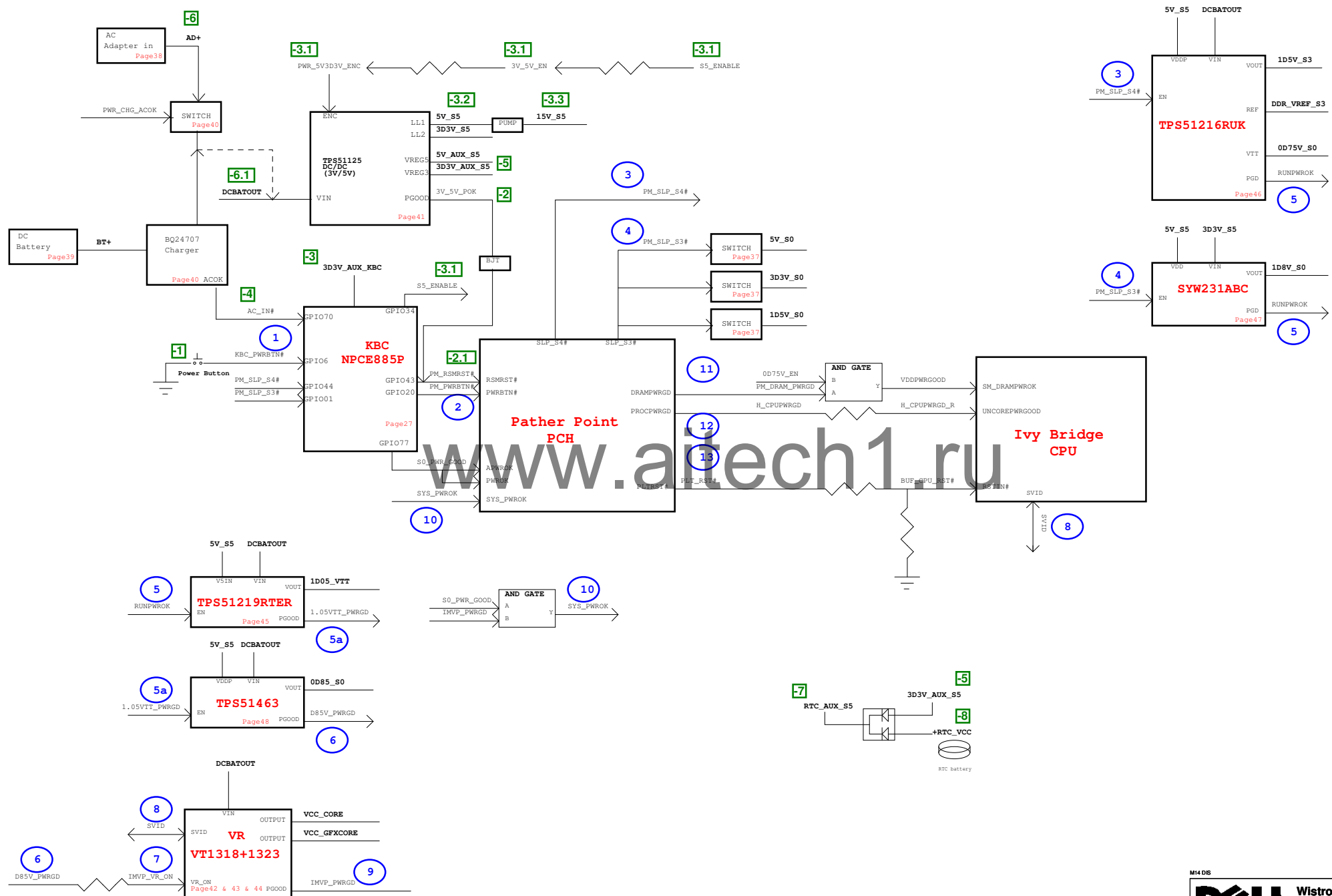
In case of a non-Deep 24/55 Platform
timing t42 should be added to t07
which will make it 100ns minimum.

VSREF must be powered up before Vcc1_3, or after Vcc1_3 within 0. V. Also, VSREF must power down after Vcc1_3, or before Vcc1_3 within 0.7 V.

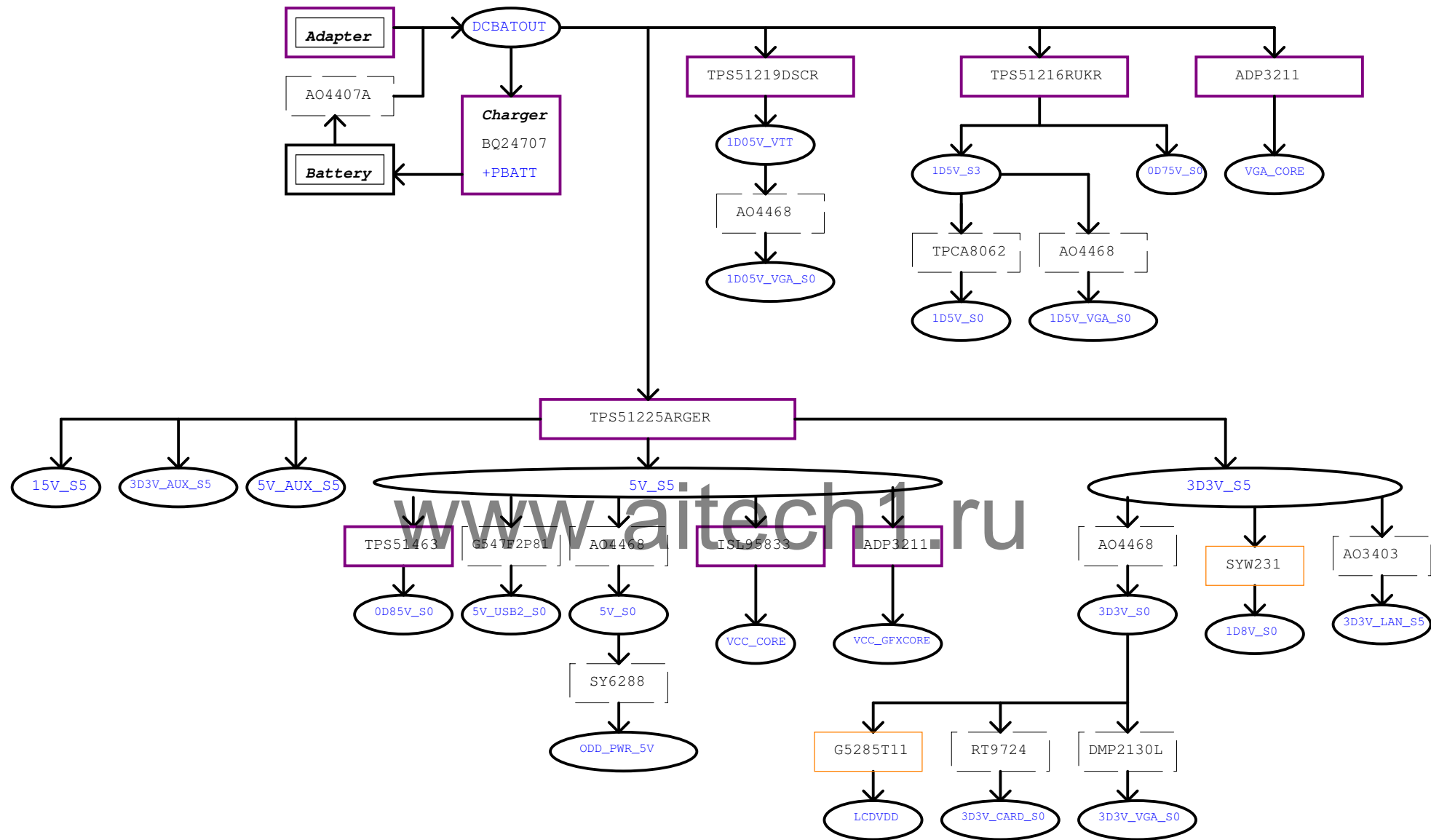
This signal represents the Power Good for all the non-CORE and non-graphics power rails.



OAK14 Chief River POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13



Power Shape

Regulator

LDO

Switch

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Title

Power Block Diagram

Size
A3

Document Number

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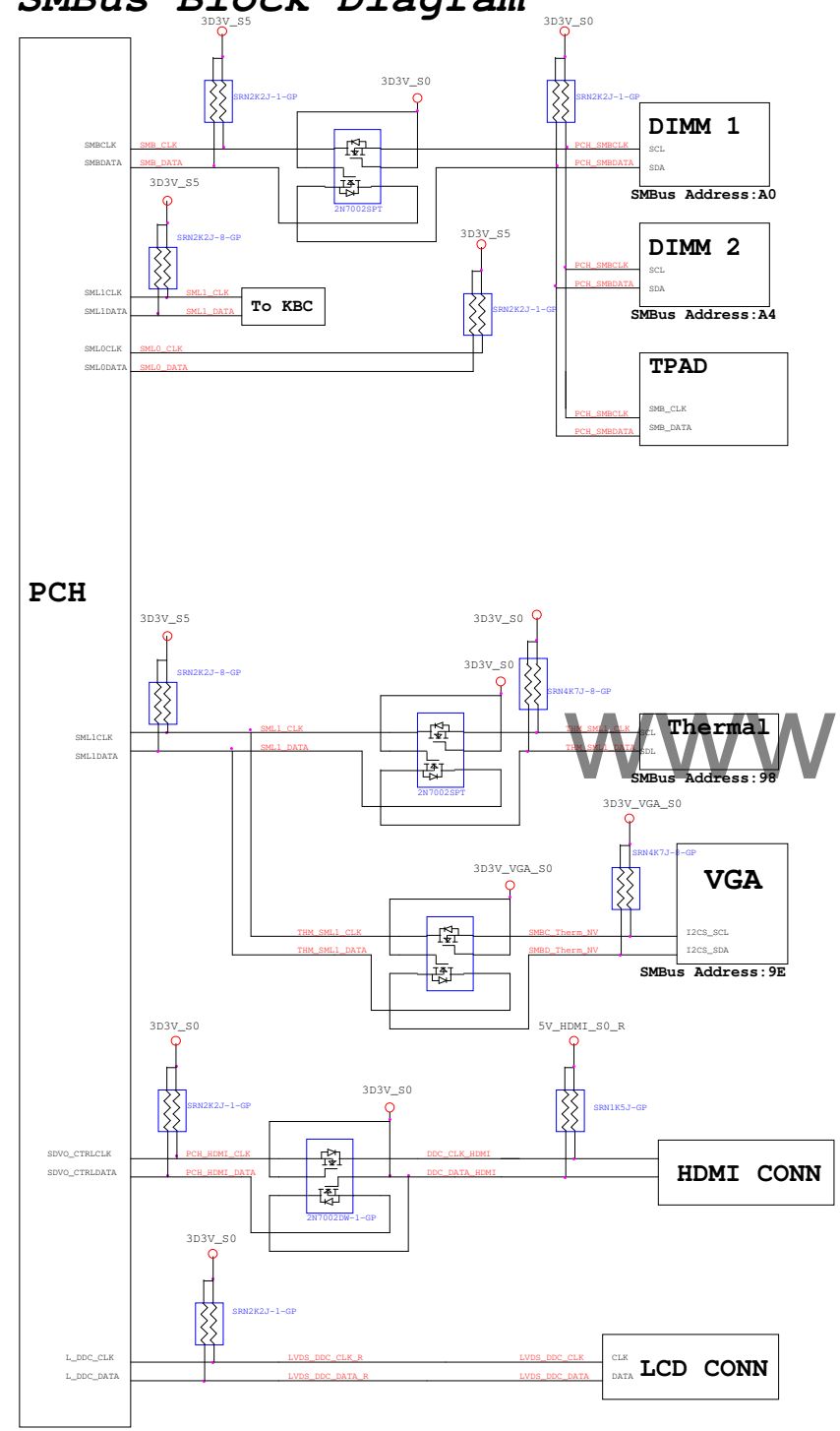
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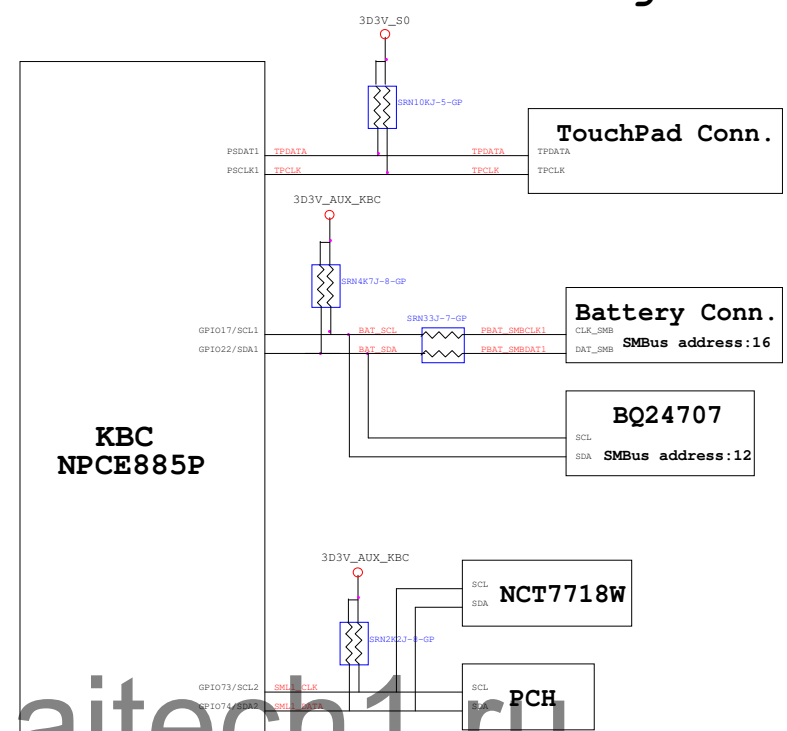
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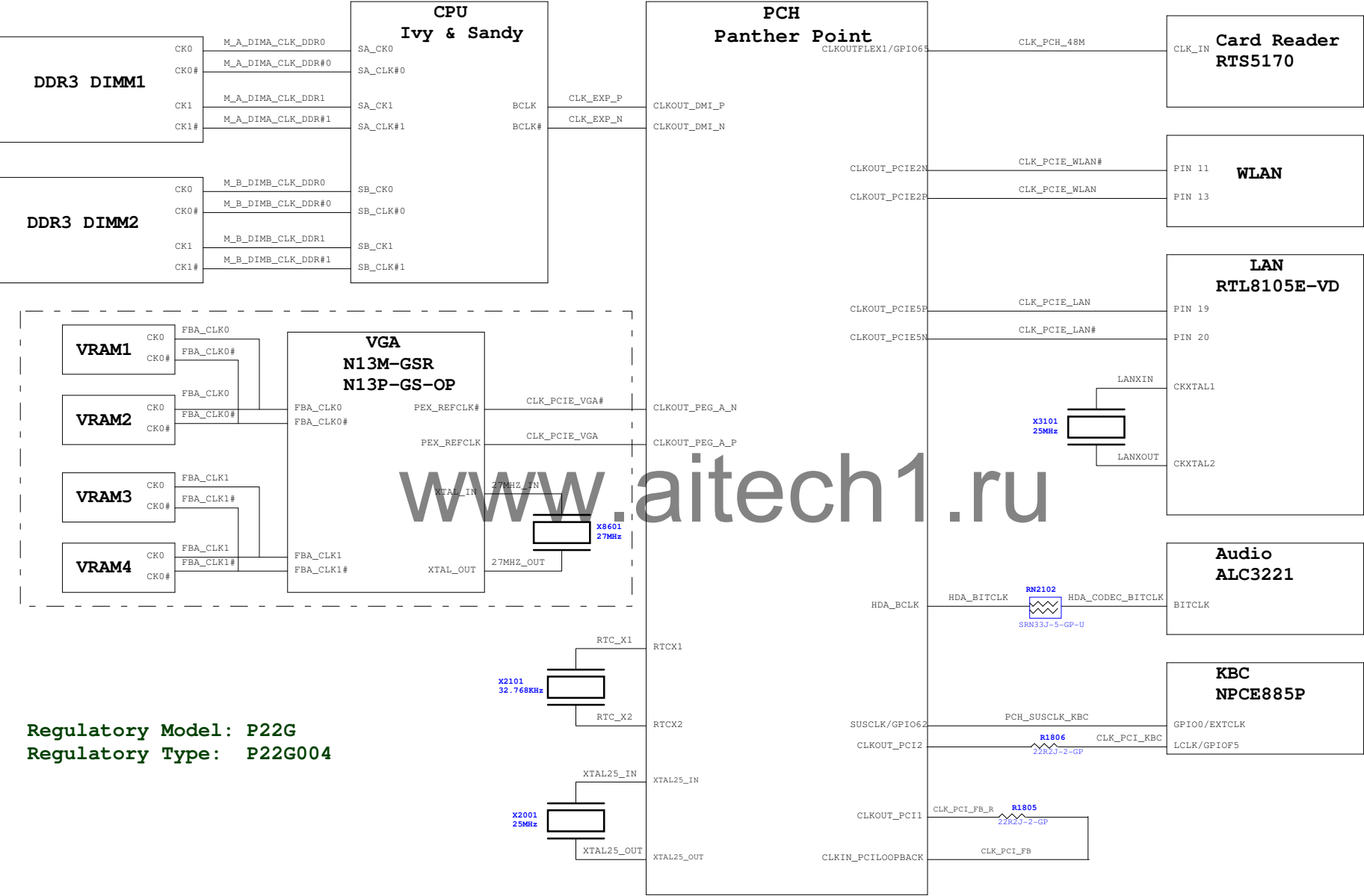
PCH SMBus Block Diagram



KBC SMBus Block Diagram

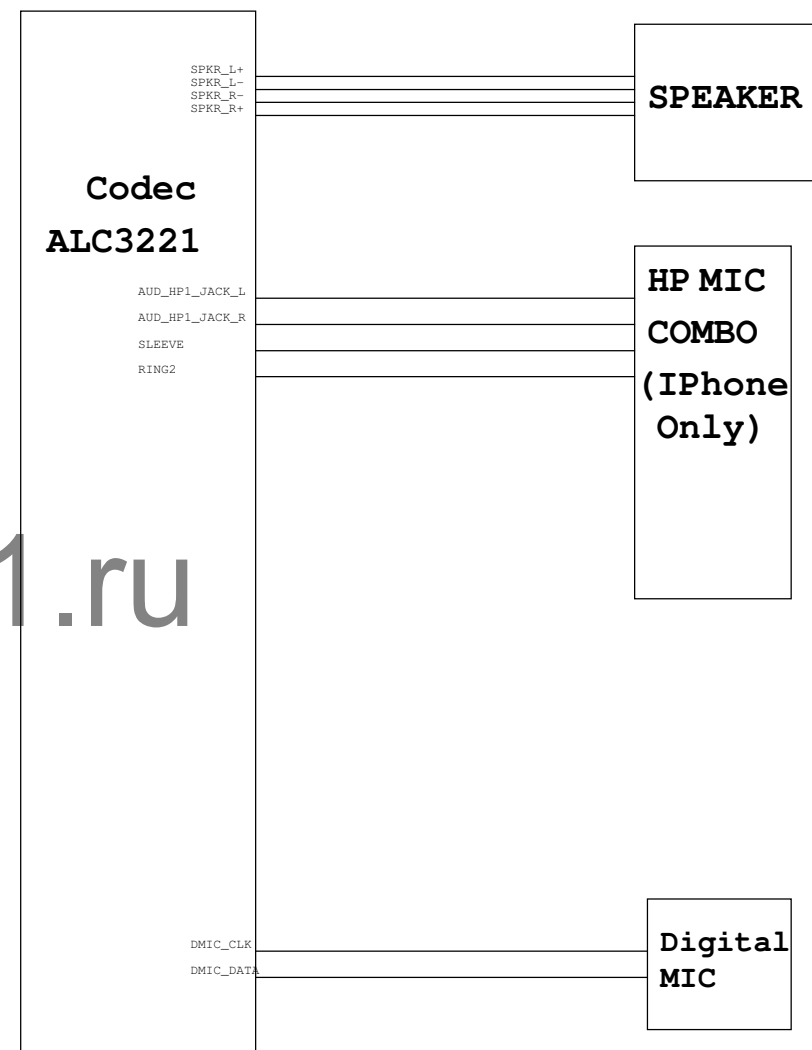


OAK14 DIS CLK Block Diagram




Regulatory Model: P22G
Regulatory Type: P22G004

Audio Block Diagram



Version	Date	PAGE	Description of Required Change
X01	5/10	P38	Dummy R3818 R3813 for DT Mode
X01	5/10	P20	Change CLK_PCIE_WLAN_REQ# PU from 3D3V_S5 to 3D3V_S0 & change port 3 to port 2(non AOAC)
X01	5/10	P86	Dummy R8613 (for N13M-GS1 strappin)
X01	5/28		Update connector list(5/28) for X01
X01	5/30	P49	Add TPNL1 (USB20 port#3)
X01	5/30	P29	Add delay circuit for Audio Jack JD pin
X01	5/30	P59	Change RJ45 Conn
X01	6/1	P38	Stuff PQ3801 PR3814 PR3815 for DT mode
X01	6/1	P37	Change R3713 to 10k for sequence timing
X01	6/1	P31	Change R3118 to 20k for sequence timing
X01	6/1	P69	Add KBL1 and keyboard backlight function
X01	6/1	P27	Change PCB version from X00 to X01
X01	6/5	P46	Fine tune the level of 1d5v_vga_s0: PR4601 (47K -> 57.6K)
X01	6/5	P58	Add TVS at combo JACK & RJ45 for EMI request
X01	6/5	P18	Move the KB_LED_BL_DET from GPIO5 to GPIO4
X01	6/11		Implement EMI change request 6/11
X01	6/11	P27	Delete RN2702 , DY R2716, Stuff R2717 For DT Mode
X01	6/11	P21	Add VRAM detect circuit at PCH_GPIO57
X01	6/11	P51	Change D5101 to 83.00056.G11 for lower internal cap
X01	6/12	P18	Move USB2.0 from port4# to port2#
X01	6/12	P49	Modify CAMERA1 to CAM1
X01	6/13	P61	Separate the USB3.0 PWR to USB30_VCCA & USB30_VCCB
X01	6/14	P49	Add LCD Back Light control circuit from KBC GPIO33
X01	6/14	P40	implement Power team request item
X01	6/15	P31	Change C3102=C3103=18pf for Xtal vendor request
X01	6/15	P62	Modify cap value for USB30_VCCA & USB30_VCCB
X01	6/18	P69	DY the Keyboard back light parts, add R6916 for PU
X01	6/18	P61	Change TC6102 & TC6104 to 78.10710.52L; TC6103 to 79.10710.60L
X01	6/18	P20	Move WLAN from PCIE 4# to PCIE 3#
X01	6/18	P51	implement EMI team request item (6/15)
X01	6/18	P69	Remove R6916 Stuff R6912
X01	6/18	P69	Change Q6801~Q6805 & Q6902 to 84.00144.P11

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